

LCFC Confidential

GS454/GS554 NM-D031 MB

Schematics Document

ICL U42 With DDR4+

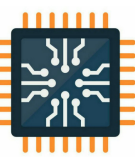
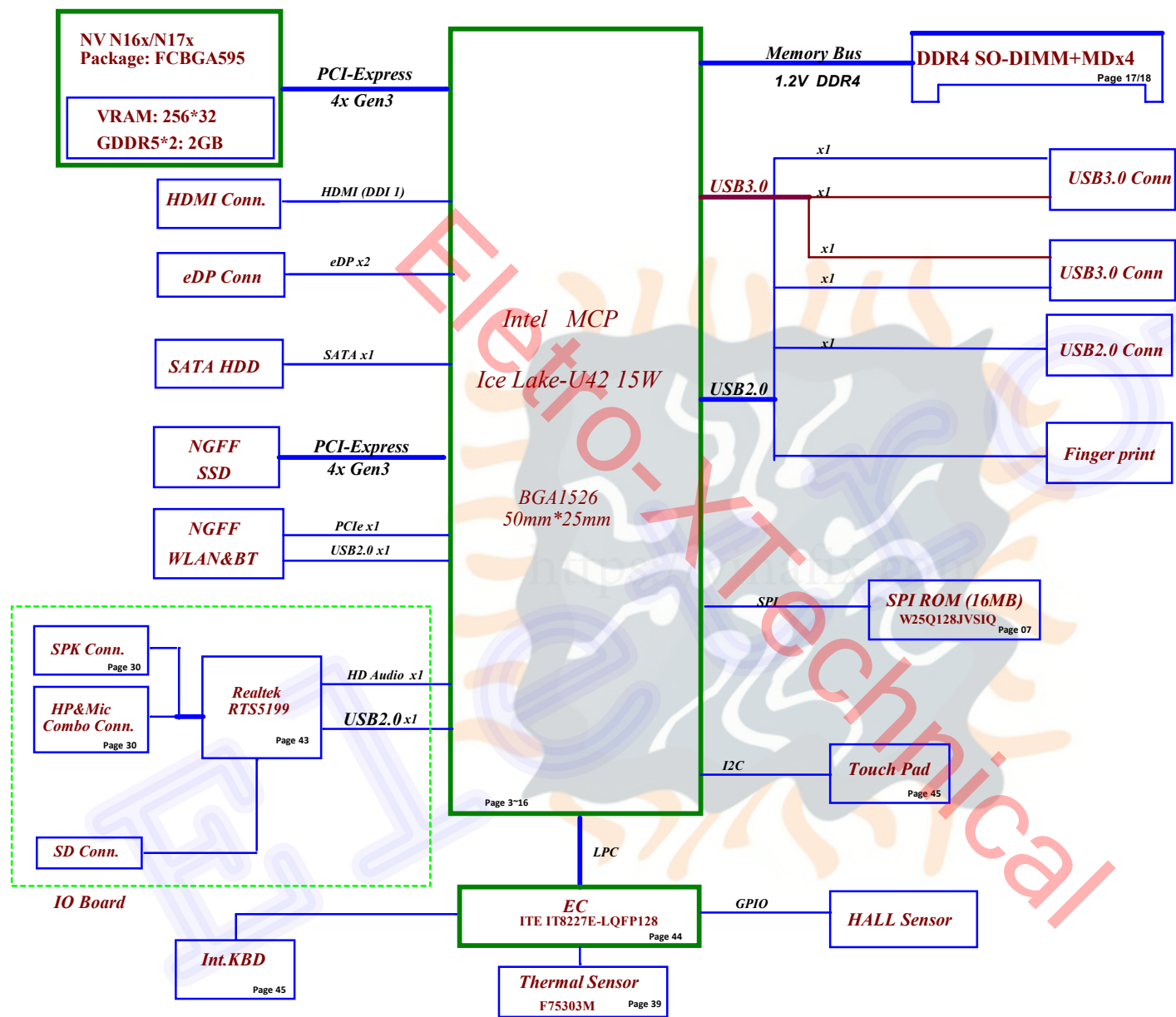
Nvidia N16V-GM

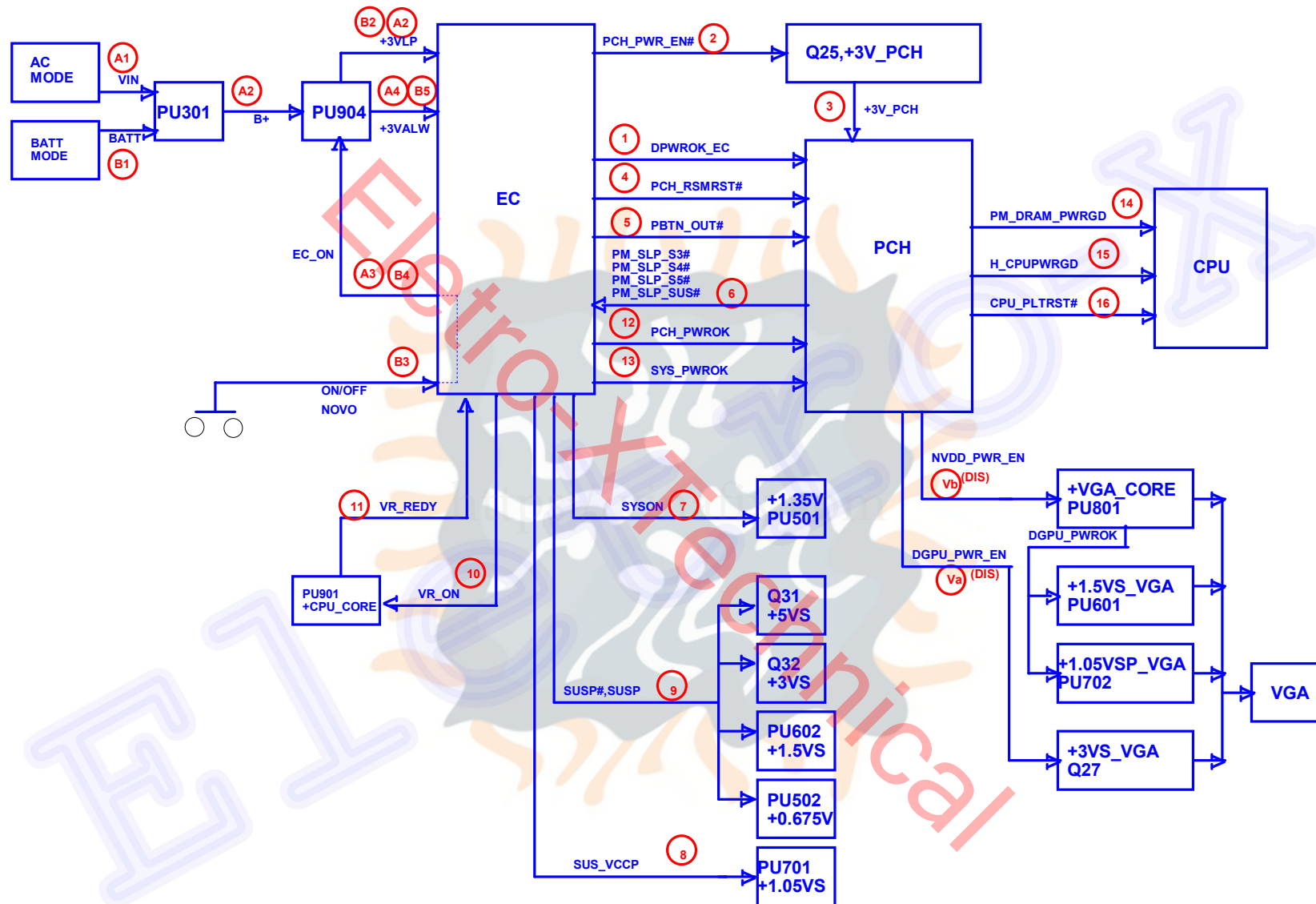
2019-10

REV:1.0

Security Classification	LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Cover Page
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</small>				Rev 0.1
Date: Friday, December 06, 2019			Sheet 1 of 60	LCFC

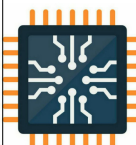
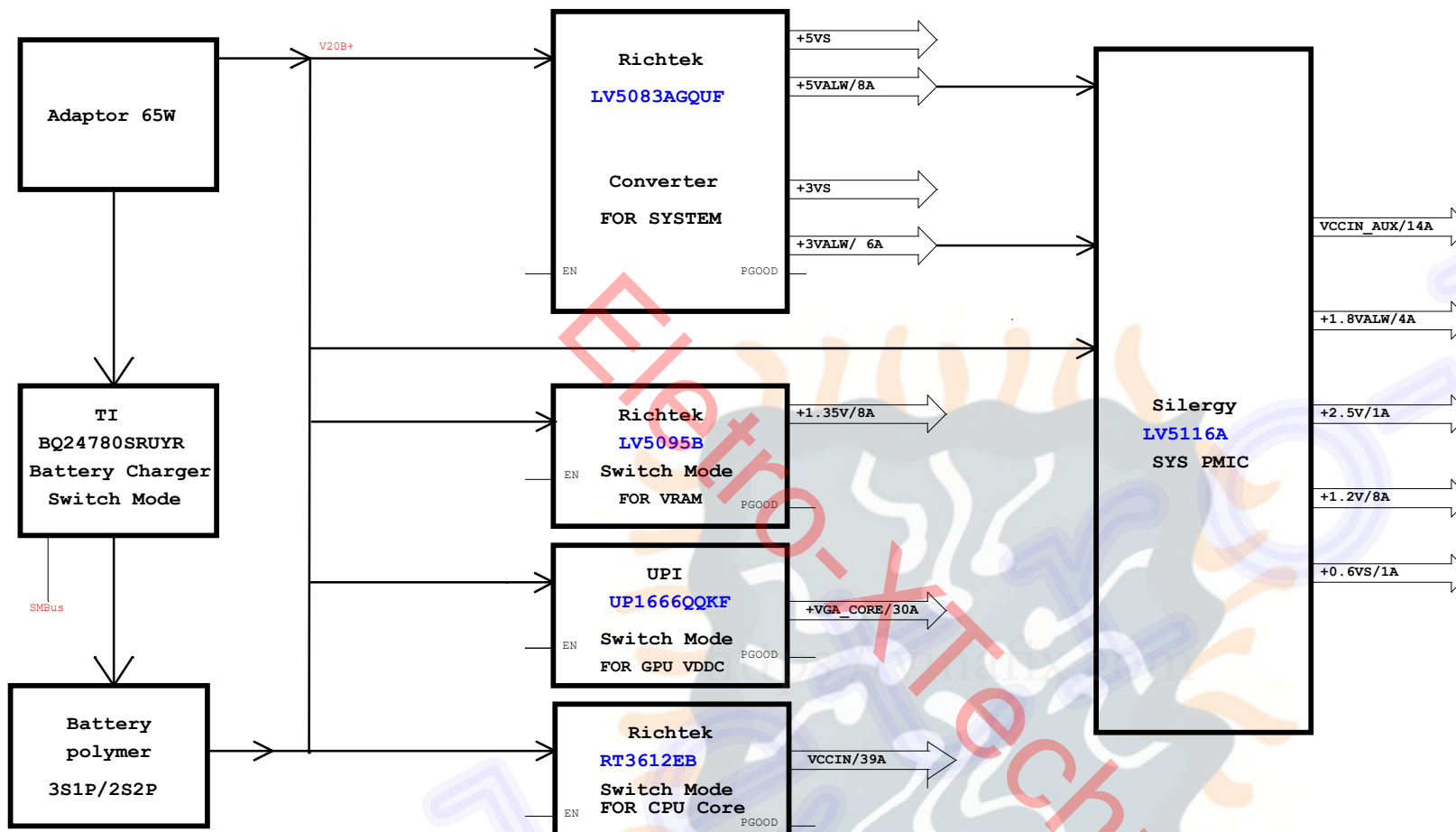






Security Classification			
LC Future Center Secret Data			
Issued Date	2015/08/20	Deciphered Date	2016/08/20
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.			

Title	
Power sequence block	
Size	Custom
Document Number	GS44D/GS54D
Date	Friday, December 06, 2019
Sheet	47 of 6



Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V9B+	+3VALW +5VALW +3VALW_PCH +1.8VALW VCC_AUX	+1.2V +2.5V_DDR +VCCST +VCCSTG	+5VS +3VS +1.8VS +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT		Function
USB3.0	1	USB3.0 Conn
	2	USB3.0 Conn
	3	NC
	4	NC
	5	
	6	
USB2.0	1	USB3.0 Conn
	2	USB3.0 Conn
	3	NC
	4	NC
	5	Camera
	6	Touch Screen
	7	Finger Print
	8	Card Reader
	9	USB2.0 conn
	10	Bluetooth
PCIE	5-8 X4	DGPU
	9	WLAN
	10	NC
	11	SATA HDD
	12	NC
	13-16 X4	PCIE/SATA SSD

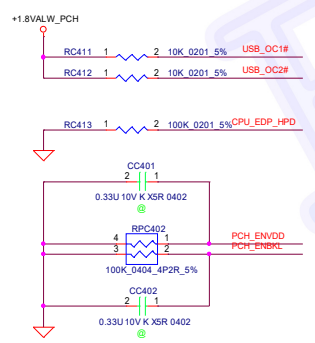
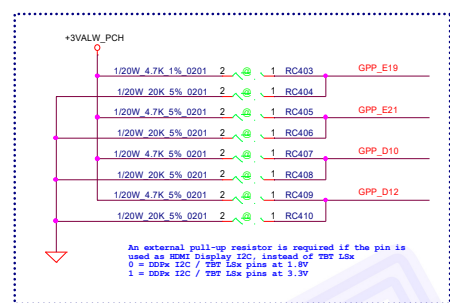
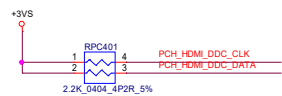
BOM Structure	BTO Item
@	Un-stuff
14@	For 14" part
15@	For 15" part
CD@	For cost down
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC un-stuff part
ME@	For ME part
UMA@	For UMA part
OPT@	For NV GPU part
OPTN16@	For NV N16S-GTR GPU part
OPTN17@	For NV N17S-G1 GPU part
TS@	For touch screen part
TP@	For TOUCH Pad Part

SMBUS Control Table

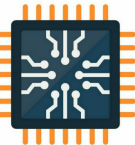
	SOURCE	BATT	Charger	DGPU	IT8227E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8227E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK0 EC_SMB_DA0	IT8227E +3VS	X	X	V +3VG_AON	V +3VS	X	X	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8227E +3VAWL	X	X	X	V	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	X

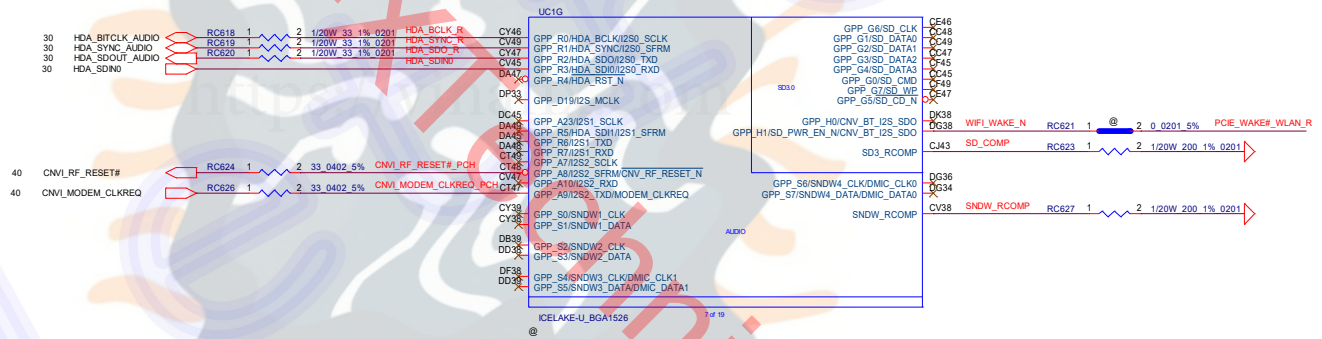
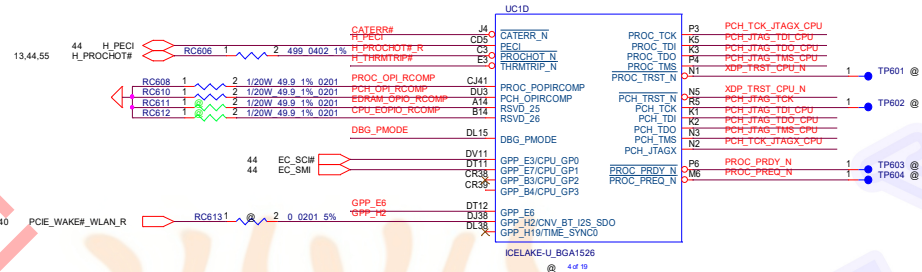
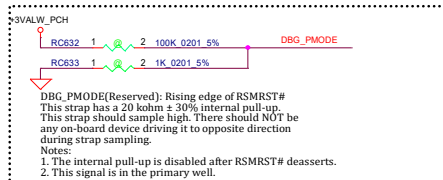
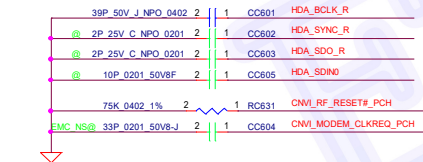
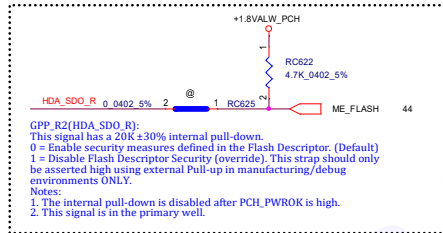
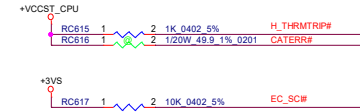
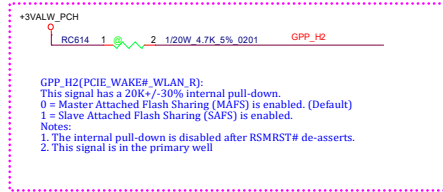
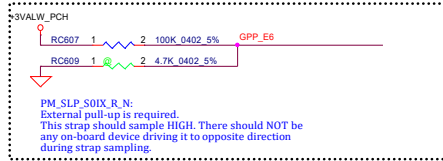
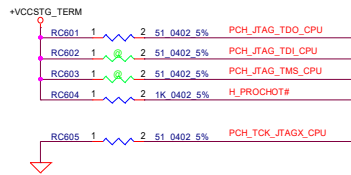
EC SMBus1 address		EC SMBus2 address		EC SMBus3 address		PCH SM Bus address	
Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	need to update	Thermal Sensor(NCT7718W)	1001_100xb	PMIC	need to update	DDR4 SODIMM	need to update
Charger	0001 0010 b	DGPU	need to update				

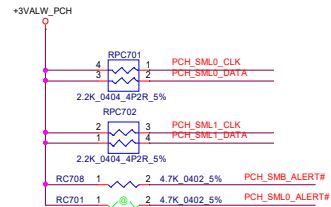
HDMI D2
HDMI D1
HDMI D0
HDMI CLK



GPIO Group	Power Supply
GPP_A	1.8V
GPP_B/C/D/E	3.3V
GPP_F	1.8V(only)
GPP_G/H	3.3V
GPP_R/S	1.8V
GPD	3.3V(only)

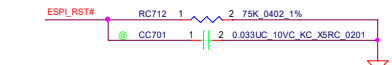
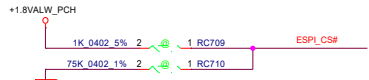




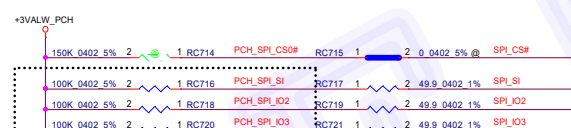


GPP_C2(PCH_SMB_ALERT#):
This signal is used to wake the system or generate SMIA.
External Pull-up resistor is required. Rising edge of RSMRST#
This signal has a 20K+/-30% internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS)
cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS)
cipher suite (with confidentiality). Must be
pulled up to support Intel AMT with TLS.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

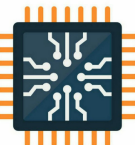
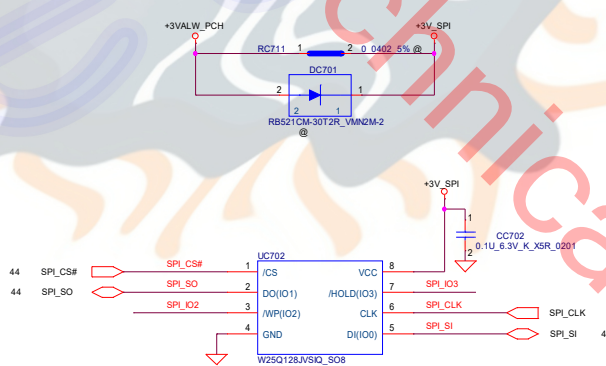
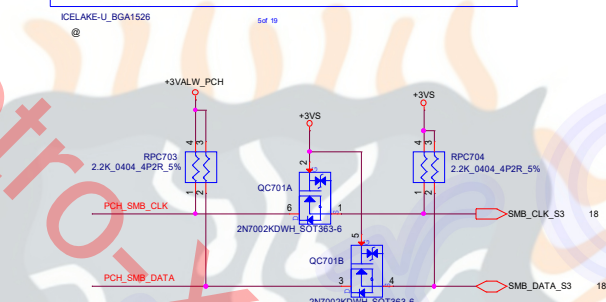
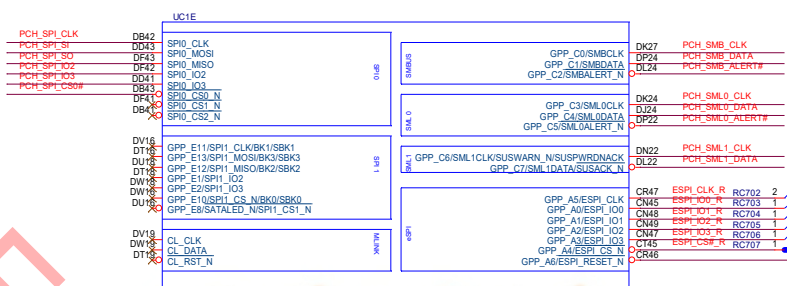
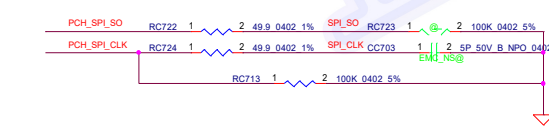
GPP_C5(PCH_SML0_ALERT#):
Rising edge of RSMRST#
This signal has a 20K+/-30% internal pull-down.
0 = Enable eSPI (Default)
1 = Disable eSPI.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

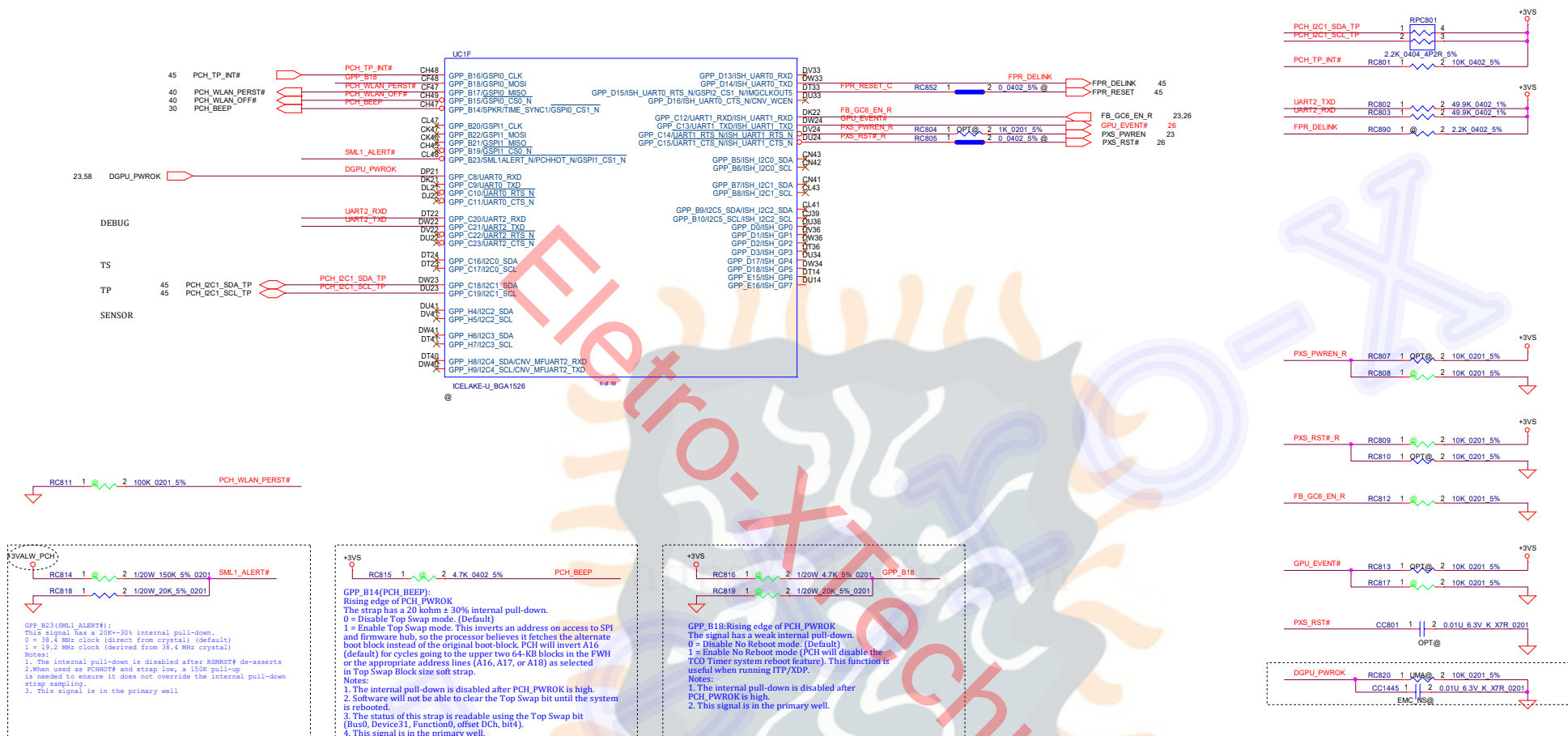


Vinafix.com

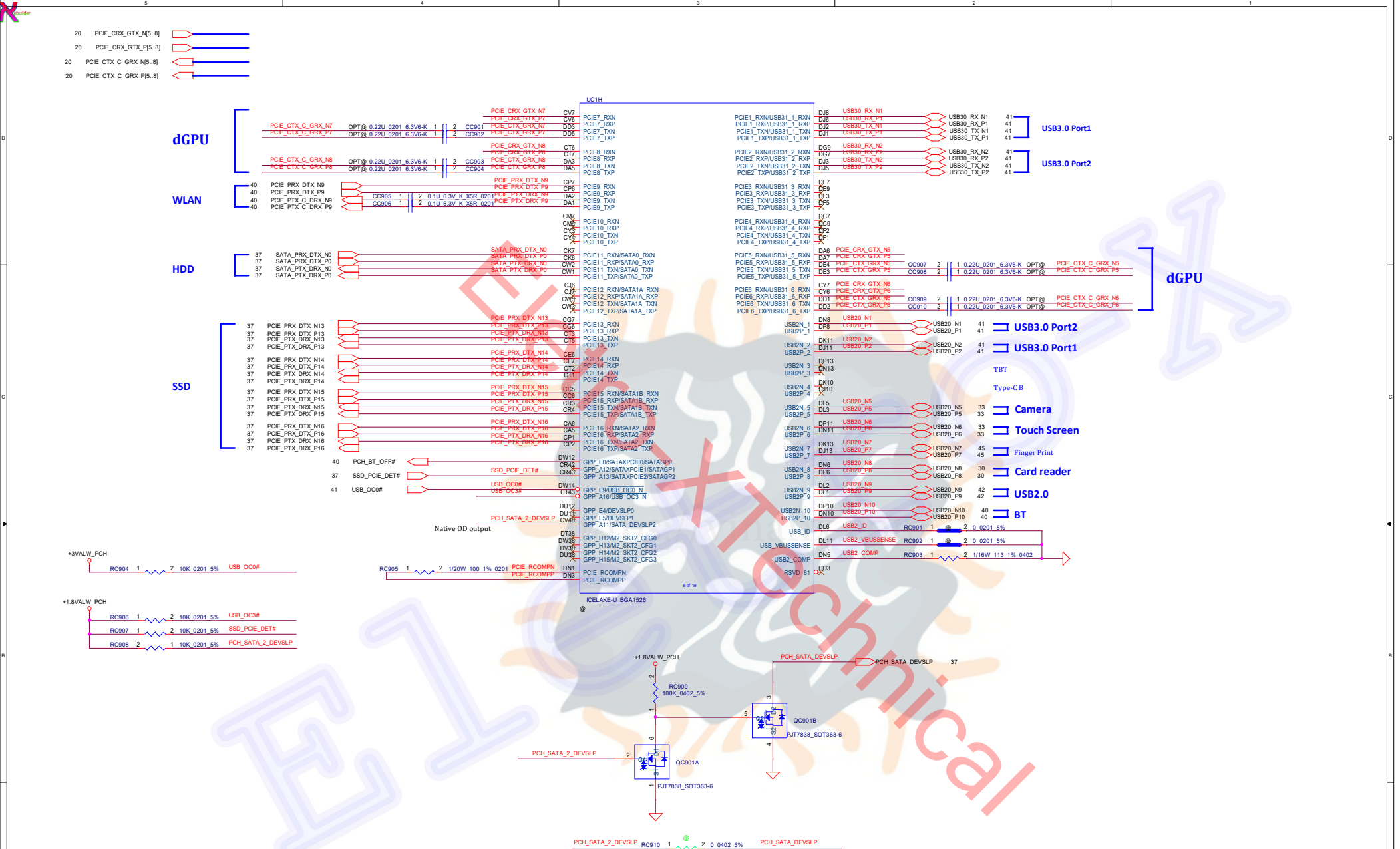


PCH_SPI_SI / PCH_SPI_WP#(IO2) / PCH_SPI_HOLD#(IO3):
External pull-up is required. Recommend 100K if pulled
up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be
any on-board device driving it to opposite direction
during strap sampling.

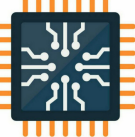
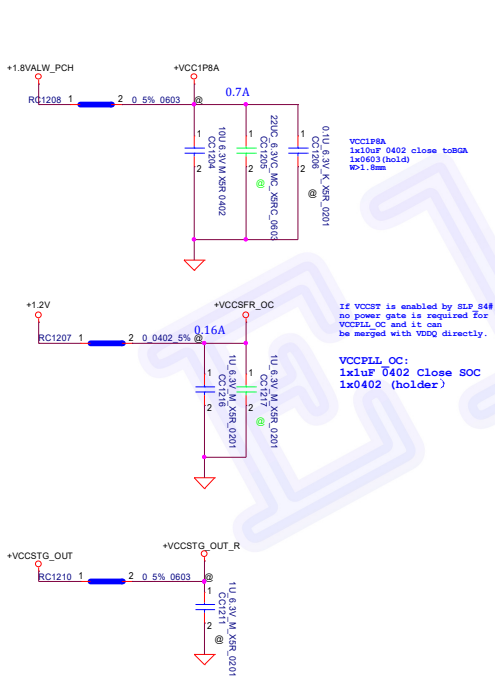
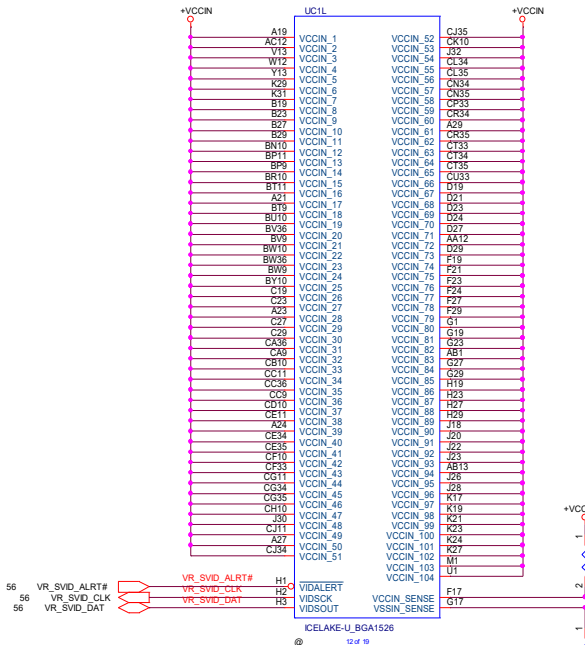
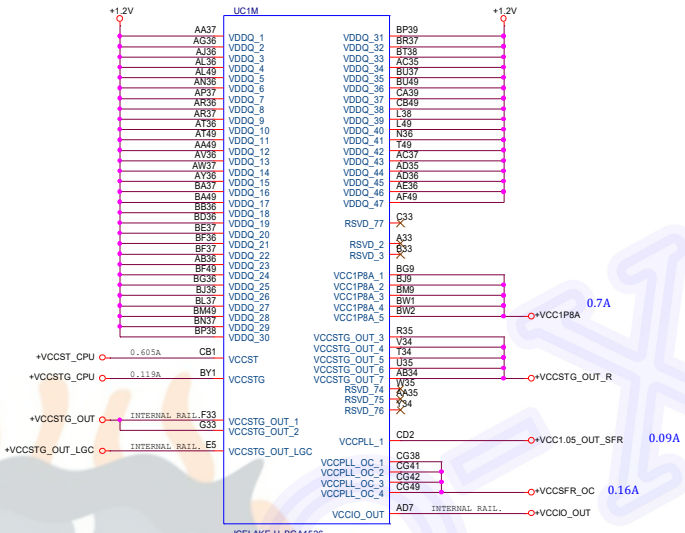
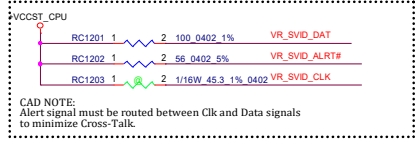




1. DEVSLP is an open-drain pin on the PCH side and is not required external pull-up or pull-down. The PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
2. DEVSLP is supported in direct connect, mSATA/mPCIe, uSSD, M.2.
3. 1 DEVSLP pin is required to support EACH DEVSLP enabled RAID storage device.
(Example: 2 DEVSLP pins are required to support 2 DEVSLP RAID storage devices).



Eletro-X Technical



UC10		
A11	VSS 1	AF45
A46	VSS 2	AF47
BA45	VSS 3	AG1
BA47	VSS 4	AG11
BB11	VSS 5	AG3
BB3	VSS 6	AG38
BB7	VSS 7	AG39
BC37	VSS 8	AG41
BC3	VSS 9	AG42
BD38	VSS 10	AG43
BD39	VSS 11	AG5
BD41	VSS 12	AG9
BD42	VSS 13	AH2
BD43	VSS 14	AH2
BD45	VSS 15	AH45
BD49	VSS 16	AH49
BD6	VSS 17	AJ2
BD6	VSS 18	AJ3
BD7	VSS 19	AJ34
BE1	VSS 20	AK37
BE2	VSS 21	AL2
BF3	VSS 22	AL45
BF45	VSS 23	AL47
BF45	VSS 24	AL6
BF47	VSS 25	AM2
BF7	VSS 26	AM37
BC3	VSS 27	AN2
BC41	VSS 28	AN38
BC7	VSS 29	AN39
BC37	VSS 30	A36
BJ1	VSS 31	AN41
BJ2	VSS 32	AN42
BJ3	VSS 33	AN43
BJ4	VSS 34	AN45
BJ45	VSS 35	AN49
BJ41	VSS 36	AN6
BJ45	VSS 37	AR1
BJ49	VSS 38	AR11
BJ7	VSS 39	AR2
BM11	VSS 40	AR3
BM3	VSS 41	AR7
BM45	VSS 42	AR7
BM47	VSS 43	AR9
BM6	VSS 44	AT3
AA47	VSS 45	AT45
BM6	VSS 46	AT47
BM7	VSS 47	AT5
BP1	VSS 48	AT6
BP2	VSS 49	AT7
BP3	VSS 50	AV37
BP43	VSS 51	AV11
BP7	VSS 52	AV2
BR45	VSS 53	AV3
BR49	VSS 54	AV38
AB11	VSS 55	AV39
AB3	VSS 56	AV41
AB38	VSS 57	AV42
AB39	VSS 58	AV45
AB41	VSS 59	AV49
AT7	VSS 60	AV54
AB42	VSS 61	AV7
AB43	VSS 62	AV3
AB5	VSS 63	AA4
AB6	VSS 64	AY7
AC45	VSS 65	B17
AD49	VSS 66	B2
AD10	VSS 67	B21
AD11	VSS 68	B24
AD34	VSS 69	B3
AD37	VSS 70	B31
A3	VSS 71	B48
AE1	VSS 72	BA1
AF37	VSS 73	BA2
VSS 74	VSS 148	

ICELAKE-U, BGA1526
@

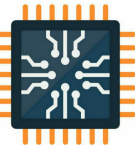
UC1P		
BT3	VSS 149	VSS 223
BT39	VSS 150	VSS 224
BT41	VSS 151	VSS 225
BT42	VSS 152	VSS 226
BT43	VSS 153	VSS 227
BT7	VSS 154	VSS 228
BU45	VSS 155	VSS 229
BU47	VSS 156	VSS 230
BU49	VSS 157	VSS 231
BV2	VSS 158	VSS 232
BV3	VSS 159	VSS 233
BV7	VSS 160	VSS 234
BW3	VSS 161	VSS 235
BW37	VSS 162	VSS 236
BW5	VSS 163	VSS 237
BW6	VSS 164	VSS 238
BW7	VSS 165	VSS 239
BV37	VSS 166	VSS 240
BV45	VSS 167	VSS 241
BV49	VSS 168	VSS 242
C11	VSS 169	VSS 243
C13	VSS 170	VSS 244
C14	VSS 171	VSS 245
C17	VSS 172	VSS 246
C21	VSS 173	VSS 247
C24	VSS 174	VSS 248
C31	VSS 175	VSS 249
C34	VSS 176	VSS 250
C36	VSS 177	VSS 251
C48	VSS 178	VSS 252
C49	VSS 179	VSS 253
CA3	VSS 180	VSS 254
CA37	VSS 181	VSS 255
CA38	VSS 182	VSS 256
CA41	VSS 183	VSS 257
CA42	VSS 184	VSS 258
CA43	VSS 185	VSS 259
CA7	VSS 186	VSS 260
CB37	VSS 187	VSS 261
CB45	VSS 188	VSS 262
CB47	VSS 189	VSS 263
CC3	VSS 190	VSS 264
CC7	VSS 191	VSS 265
CE37	VSS 192	VSS 266
CE45	VSS 193	VSS 267
CE49	VSS 194	VSS 268
CE9	VSS 195	VSS 269
CG37	VSS 196	VSS 270
CG39	VSS 197	VSS 271
CG43	VSS 198	VSS 272
CG45	VSS 199	VSS 273
CG47	VSS 200	VSS 274
CG9	VSS 201	VSS 275
CH3	VSS 202	VSS 276
CH5	VSS 203	VSS 277
CJ37	VSS 204	VSS 278
CJ42	VSS 205	VSS 279
CJ49	VSS 206	VSS 280
CK45	VSS 207	VSS 281
CK49	VSS 208	VSS 282
CK9	VSS 209	VSS 283
CL37	VSS 210	VSS 284
CL42	VSS 211	VSS 285
CL49	VSS 212	VSS 286
CM45	VSS 213	VSS 287
CM47	VSS 214	VSS 288
CM9	VSS 215	VSS 289
CN3	VSS 216	VSS 290
CN37	VSS 217	VSS 291
CN39	VSS 218	VSS 292
CN5	VSS 219	VSS 293
CP9	VSS 220	VSS 294
CR32	VSS 221	VSS 295
VSS 222	VSS 296	

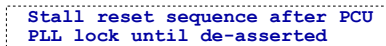
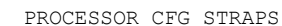
ICELAKE-U, BGA1526
@

UC1Q		
DJ33	VSS 297	VSS 362
DJ36	VSS 298	VSS 363
DJ42	VSS 299	VSS 364
DK3	VSS 300	VSS 365
DK4	VSS 301	VSS 366
DK49	VSS 302	VSS 367
DK6	VSS 303	VSS 368
DK8	VSS 304	VSS 369
DL10	VSS 305	VSS 370
DL13	VSS 306	VSS 371
DL44	VSS 307	VSS 372
DL47	VSS 308	VSS 373
DM7	VSS 309	VSS 374
DM15	VSS 310	VSS 375
DM24	VSS 311	VSS 376
DN31	VSS 312	VSS 377
DN36	VSS 313	VSS 378
DN42	VSS 314	VSS 379
DP45	VSS 315	VSS 380
DR49	VSS 316	VSS 381
DT1	VSS 317	VSS 382
DT10	VSS 318	VSS 383
DT15	VSS 319	VSS 384
DT20	VSS 320	VSS 385
DT27	VSS 321	VSS 386
DT3	VSS 322	VSS 387
DT32	VSS 323	VSS 388
DT37	VSS 324	VSS 389
DT42	VSS 325	VSS 390
DT49	VSS 326	VSS 391
DT6	VSS 327	VSS 392
DT7	VSS 328	VSS 393
DT8	VSS 329	VSS 394
DT9	VSS 330	VSS 395
DU10	VSS 331	VSS 396
DU15	VSS 332	VSS 397
DU2	VSS 333	VSS 398
DU20	VSS 334	VSS 399
DU27	VSS 335	VSS 400
DU32	VSS 336	VSS 401
DU37	VSS 337	VSS 402
DU40	VSS 338	VSS 403
DU49	VSS 339	VSS 404
DU7	VSS 340	VSS 405
DV2	VSS 341	VSS 406
DV44	VSS 342	VSS 407
DV48	VSS 343	VSS 408
DV5	VSS 344	VSS 409
DW1	VSS 345	VSS 410
DW10	VSS 346	VSS 411
DW2	VSS 347	VSS 412
DW20	VSS 348	VSS 413
DW27	VSS 349	VSS 414
DW44	VSS 350	VSS 415
DW48	VSS 351	VSS 416
DW49	VSS 352	VSS 417
DW5	VSS 353	VSS 418
DW7	VSS 354	VSS 419
E11	VSS 355	VSS 420
E31	VSS 356	VSS 421
E36	VSS 357	VSS 422
E39	VSS 358	VSS 423
E42	VSS 359	VSS 424
E6	VSS 360	VSS 425
VSS 361	VSS 426	
VSS 427	VSS 427	

ICELAKE-U, BGA1526
@
17 of 19

Vinafix.com



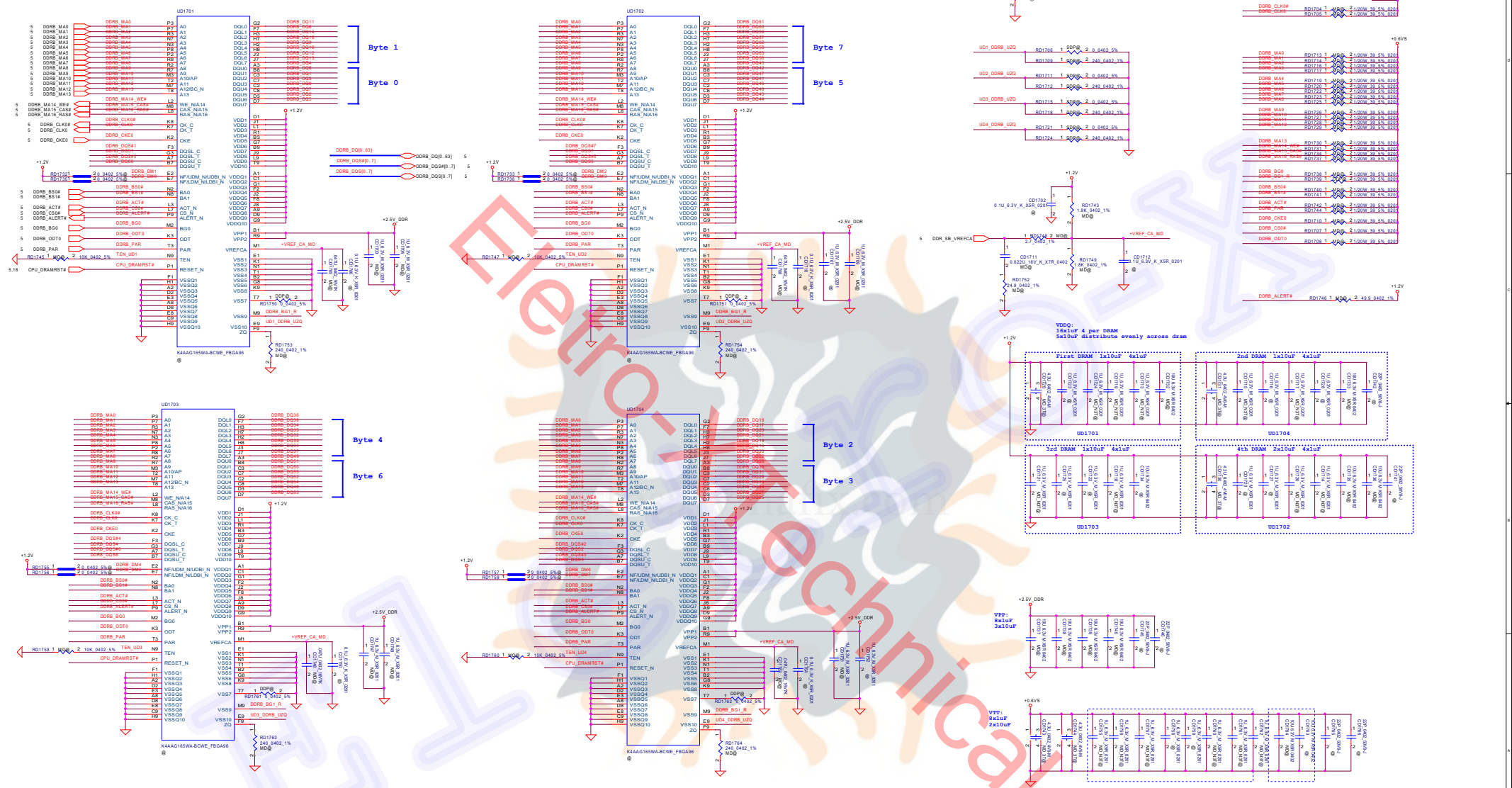
[illegible]

CFG16 RC1604 1 2 51 0402 5%
CFG18 RC1605 1 2 51 0402 5%

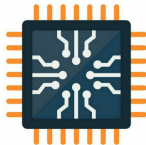


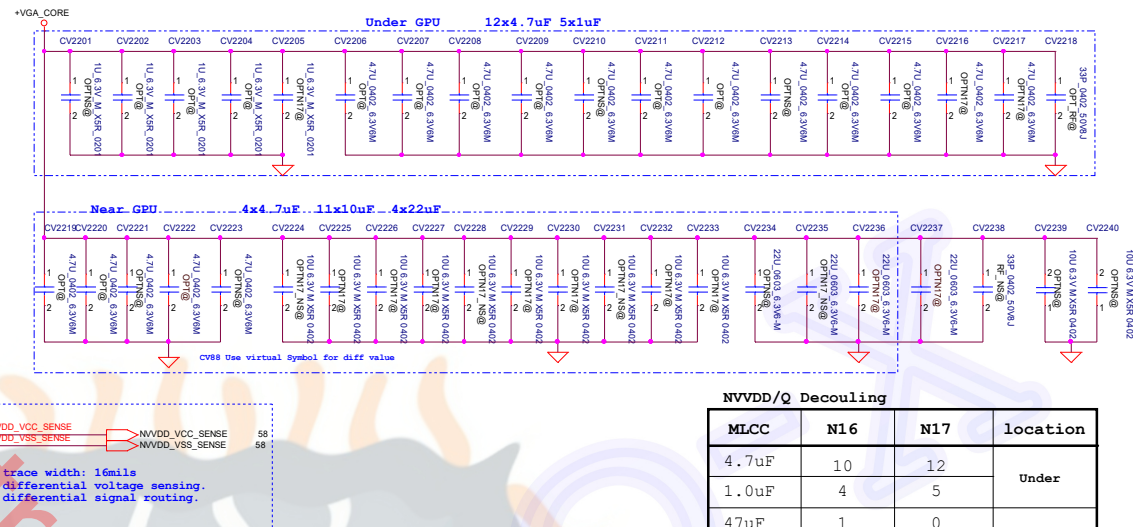
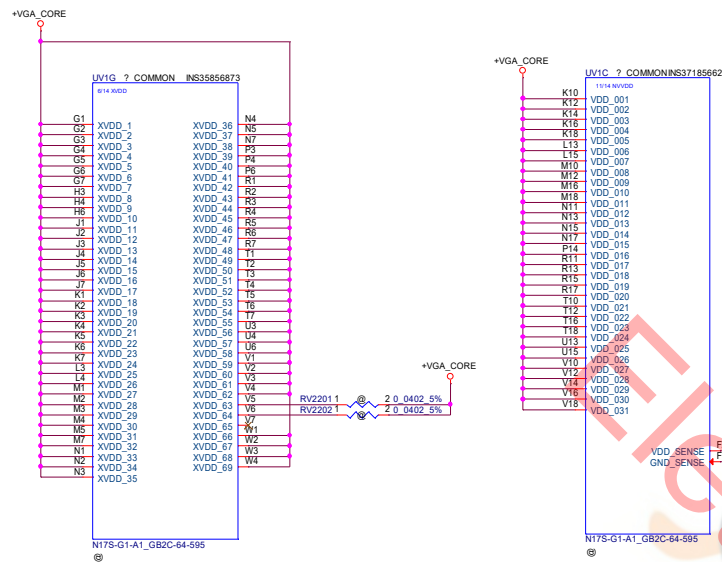


DDR4 Memory Down



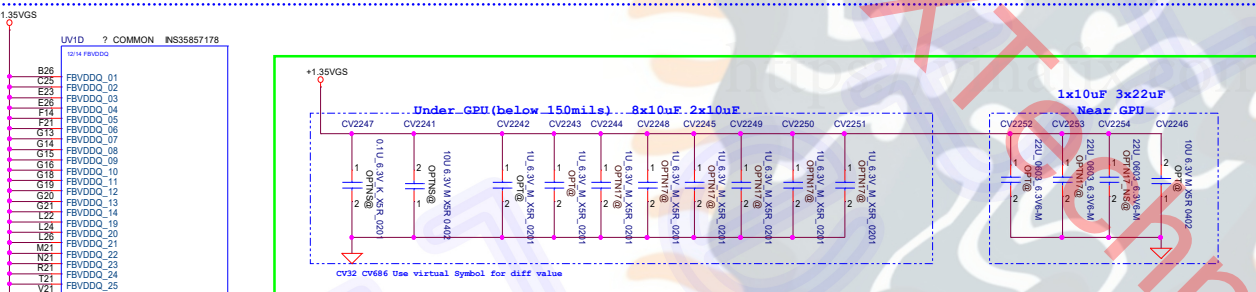
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2017/06/24	Deciphered Date	2018/06/23	DDR4 Memory Down	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE REPRODUCED FROM THE CUSTODY OF THE CONTENTS DIVISION OF IAD OR ANY OTHER IAD OR IAD DIVISION BY ANY IAD OR IAD DIVISION WITHOUT THE WRITTEN PERMISSION OF THE CONTENTS DIVISION OF IAD.				Size	Document Number
				System	GS44D/GS54D
				Page	17 of 18





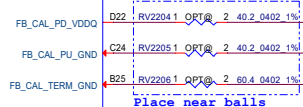
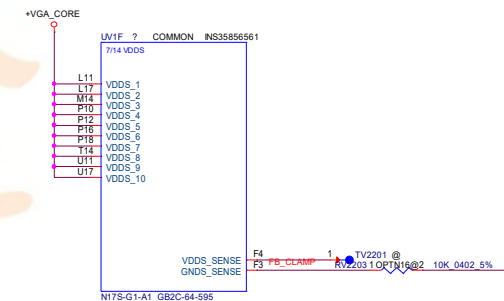
NVVDD/Q Decoupling

MLCC	N16	N17	location
4.7uF	10	12	Under
1.0uF	4	5	
47uF	1	0	Near
10uF	0	11	
22uF	1	4	
4.7uF	5	4	
330uF	1	2	

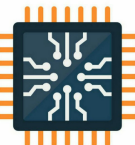


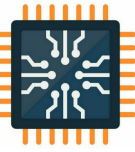
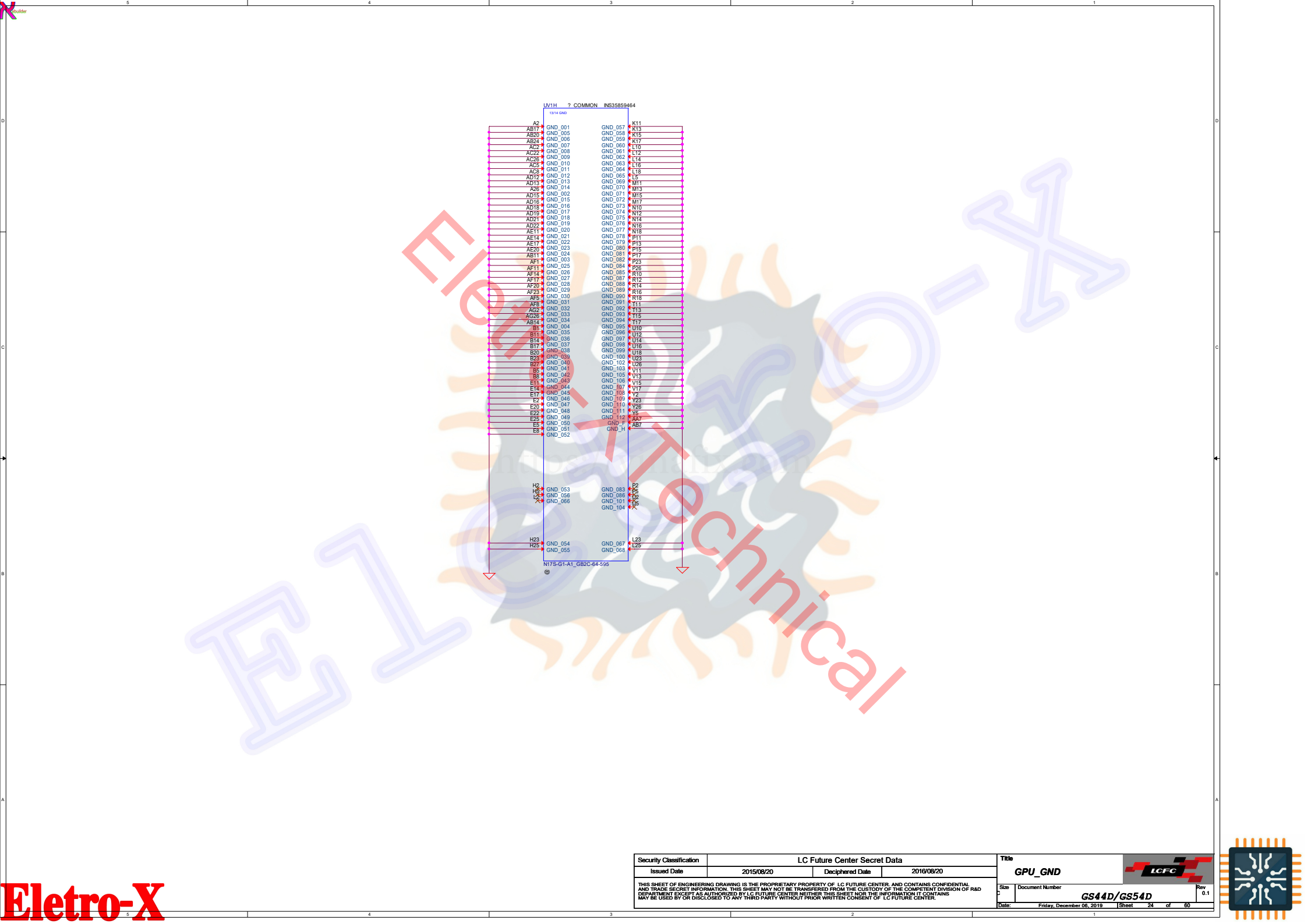
FBVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	2	0	Under
1.0uF	2	8	
4.7uF	2	0	Near
10uF	0	2	
10uF	1	1	
22uF	1	3	



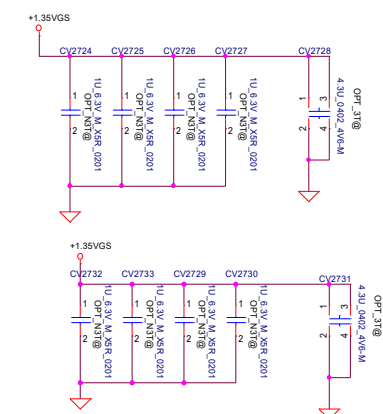
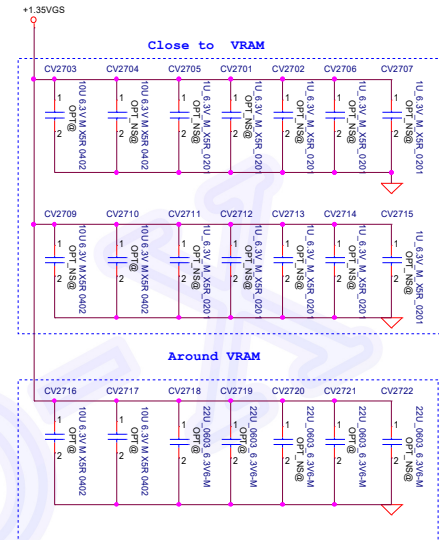
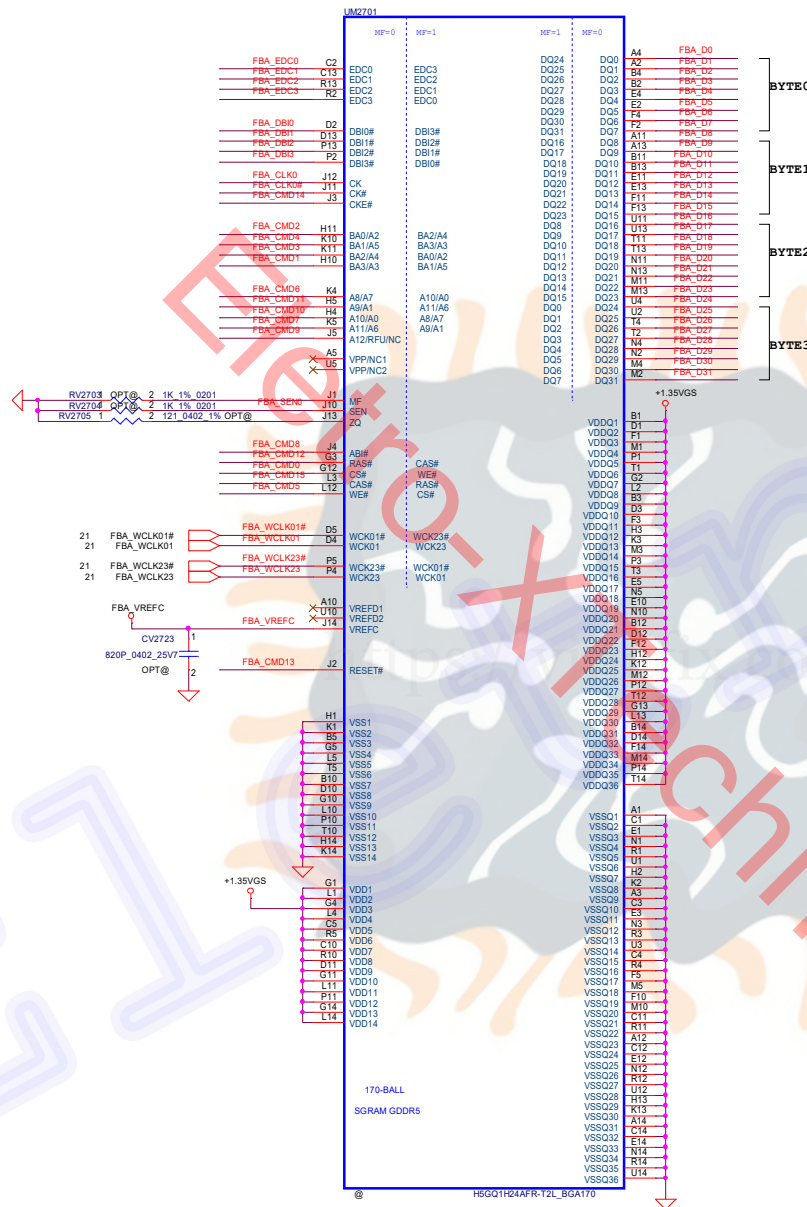
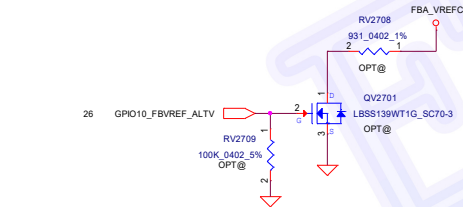
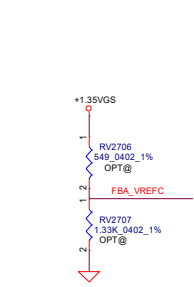
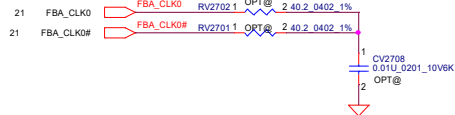
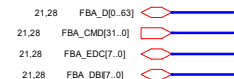
CALIBRATION PIN	GDDR5
FB_CAL x PD_VDDQ	40.2ohm
FB_CAL x PU_GND	40.2ohm
FB_CAL x TERM_GND	60.4ohm



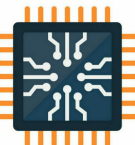


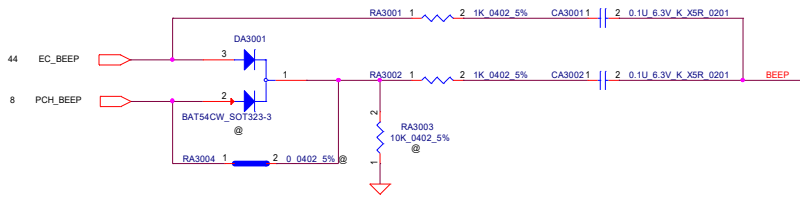
Lower 32 bits

MF=0 No Mirror

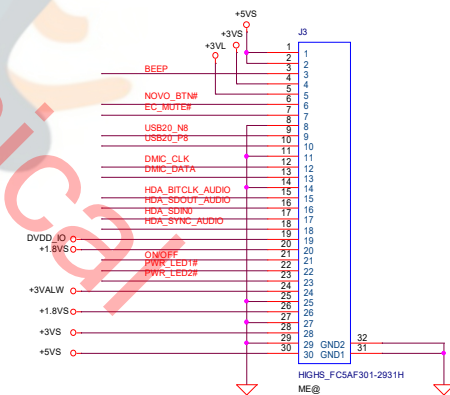
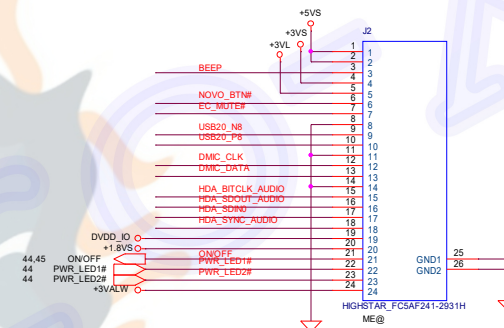
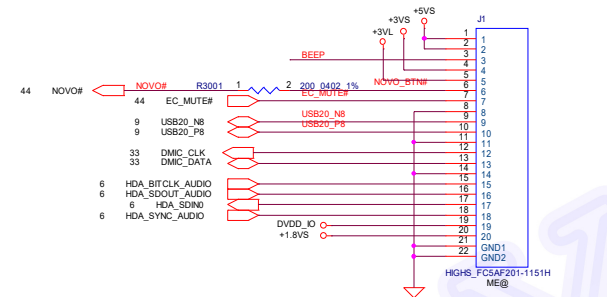
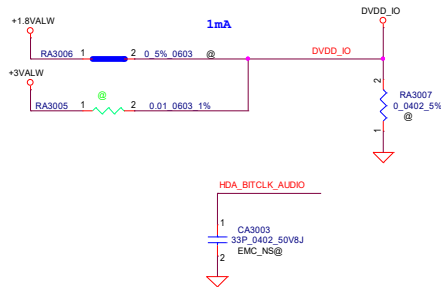


Security Classification	LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	GPU_GDDR5_Rank0_31..0
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Rev 0.1
Size				Document Number
Date				GS44D/GS54D
Friday, December 06, 2018				Sheet 27 of 80

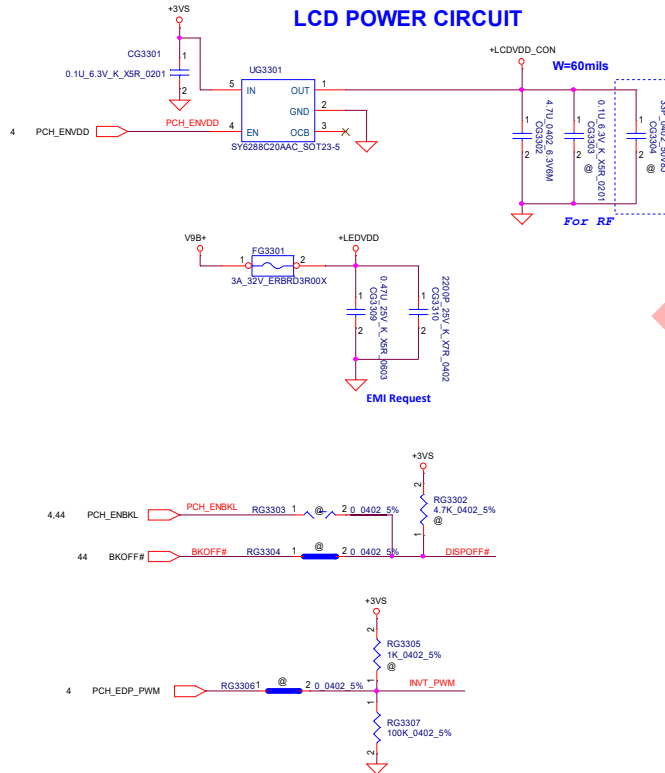




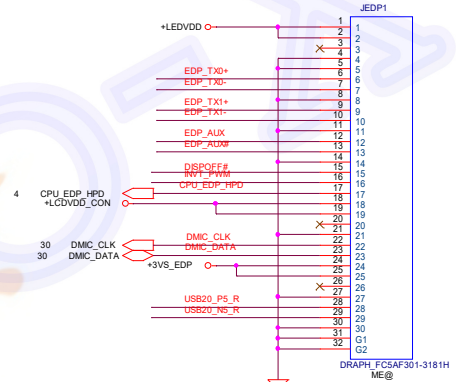
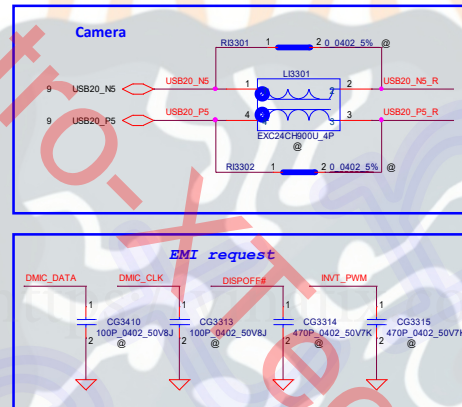
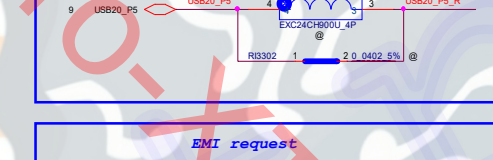
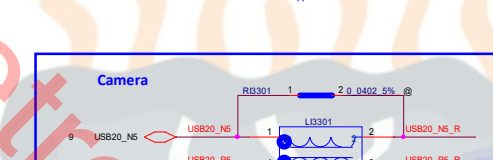
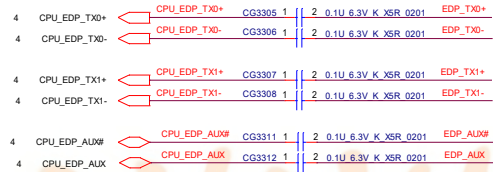
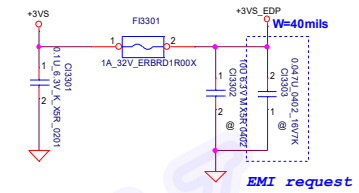
CPU HDA BUS power 1.8VALW



LCD POWER CIRCUIT

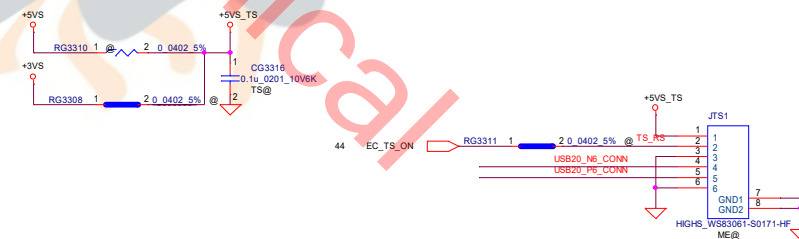
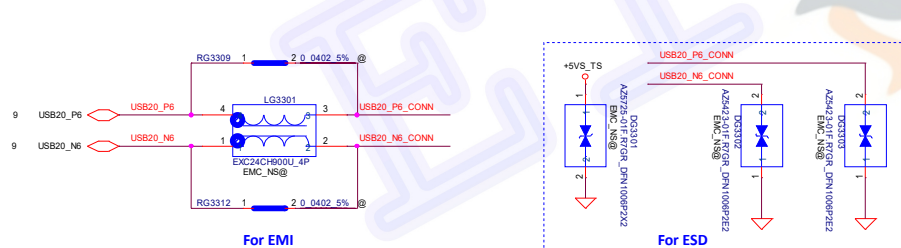


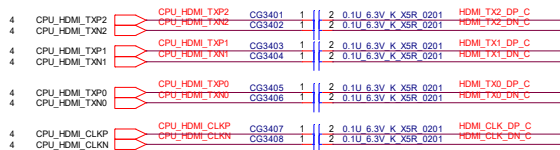
CMOS Camera



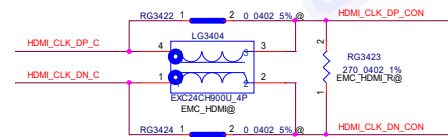
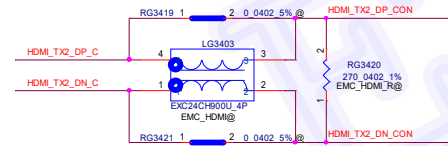
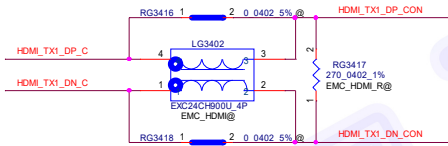
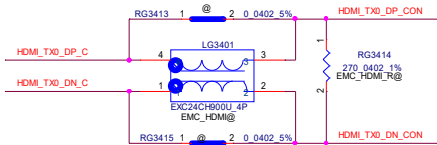
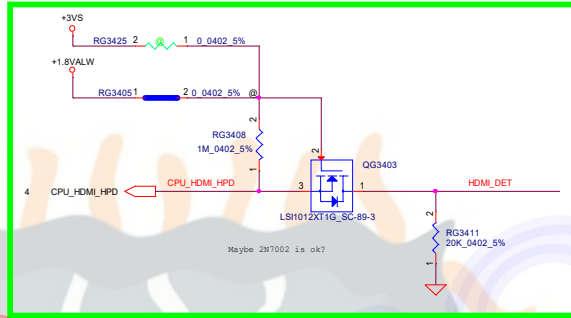
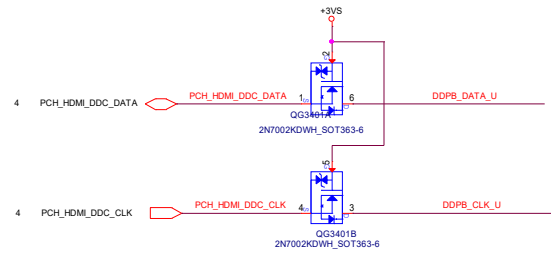
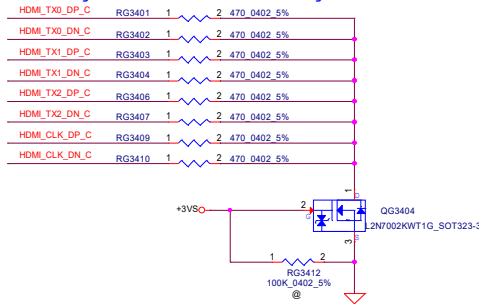
Vinafix.com

Touch Screen

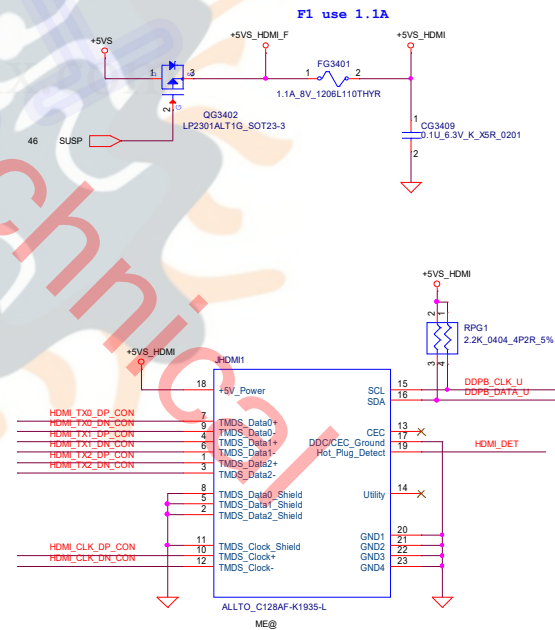
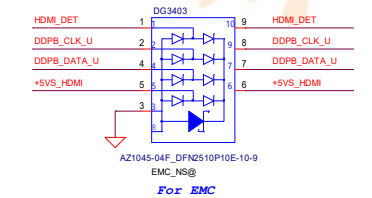
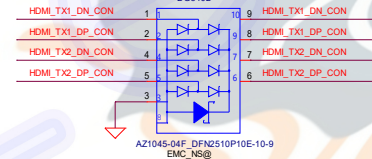
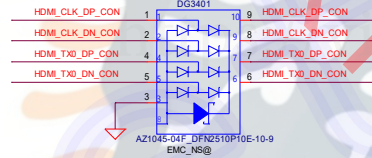




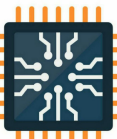
Need to change about 4700hm 5%-575412 Page115 Rev0.8



For EMC

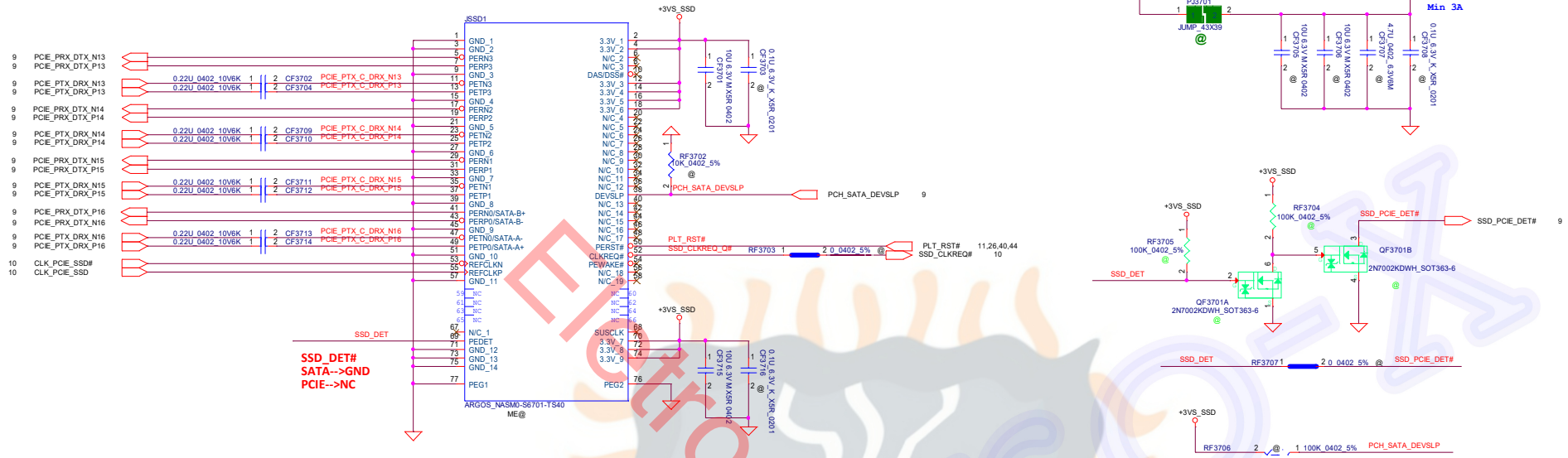


Security Classification	LC Future Center Secret Data		Title	HDMI_CONN	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Size	Document Number
THIS SHEET OF ENGINEERING DRAWINGS IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				GS44D/GS54D	
				Date	Friday, December 06, 2018
				Sheet	34 of 80

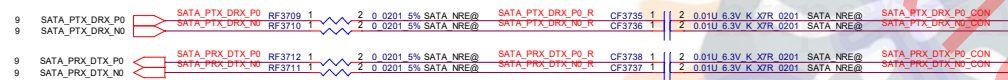


M.2 SSD

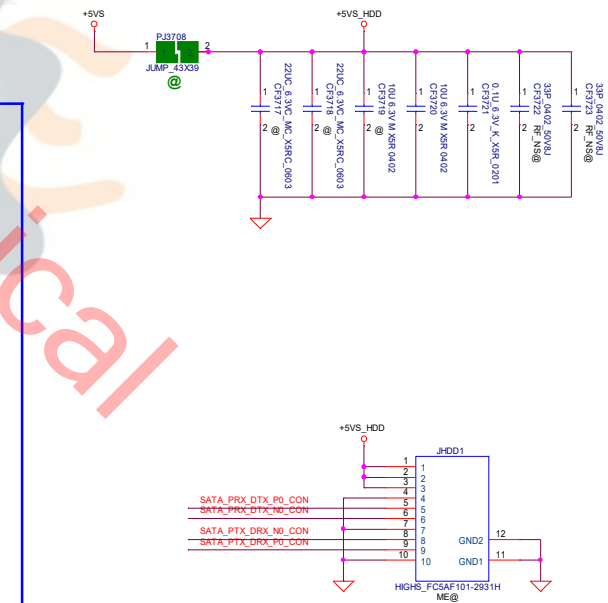
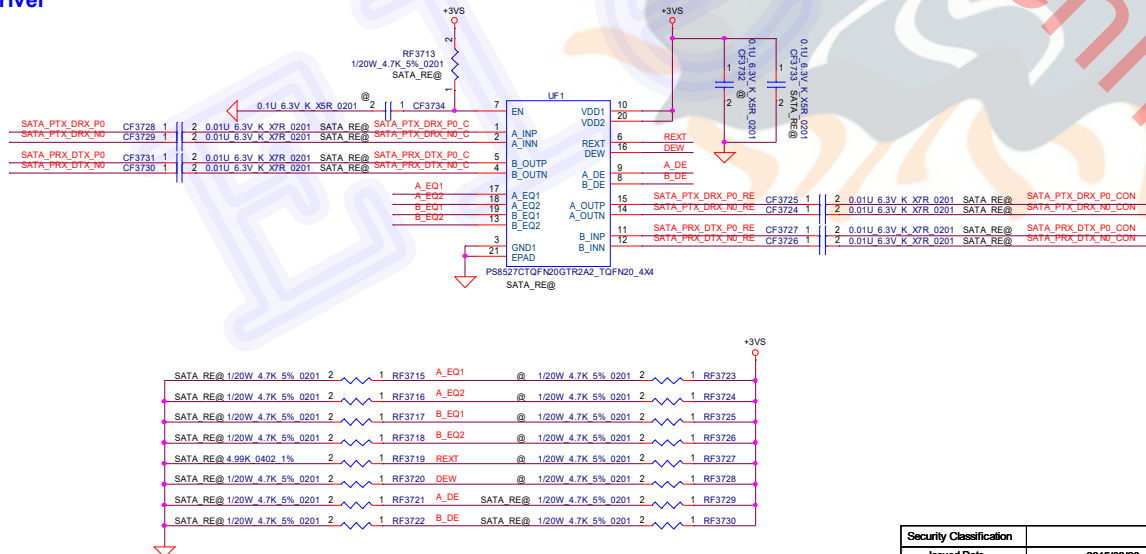
Vinafix.com



SATA



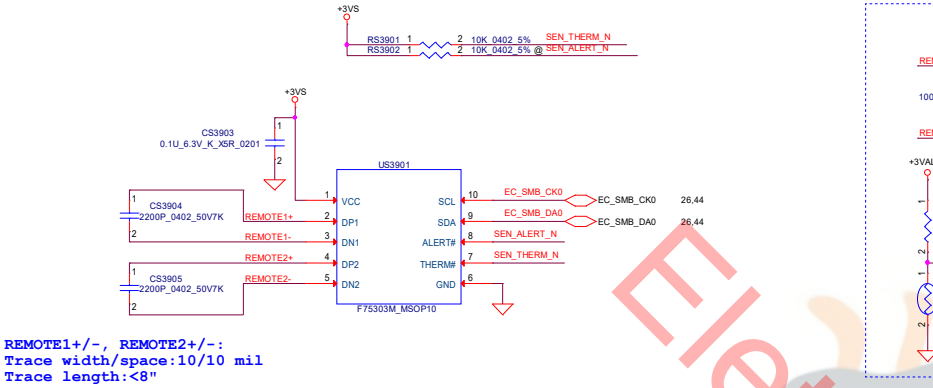
SATA Redriver



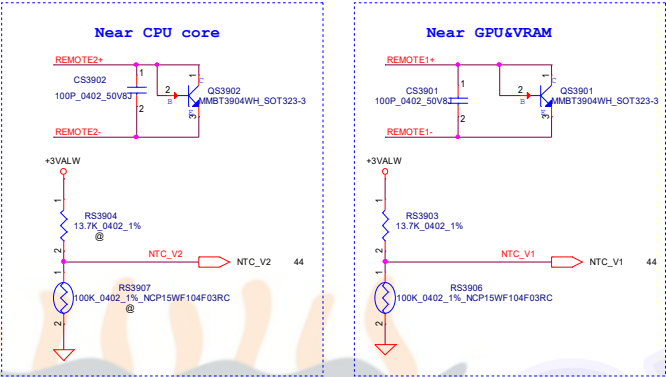
Security Classification	LC Future Center Secret Data		Title	NGFF_SSD_1	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Size	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				GS44D/GS54D	Rev 0.1
				Date:	Friday, December 06, 2018
				Sheet	37 of 60



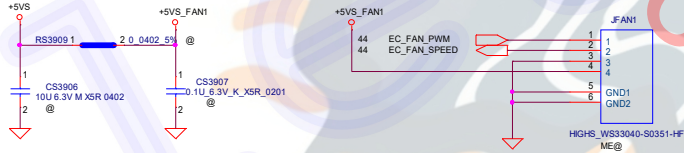
SMSC thermal sensor



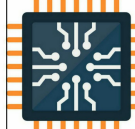
REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"




FAN Conn

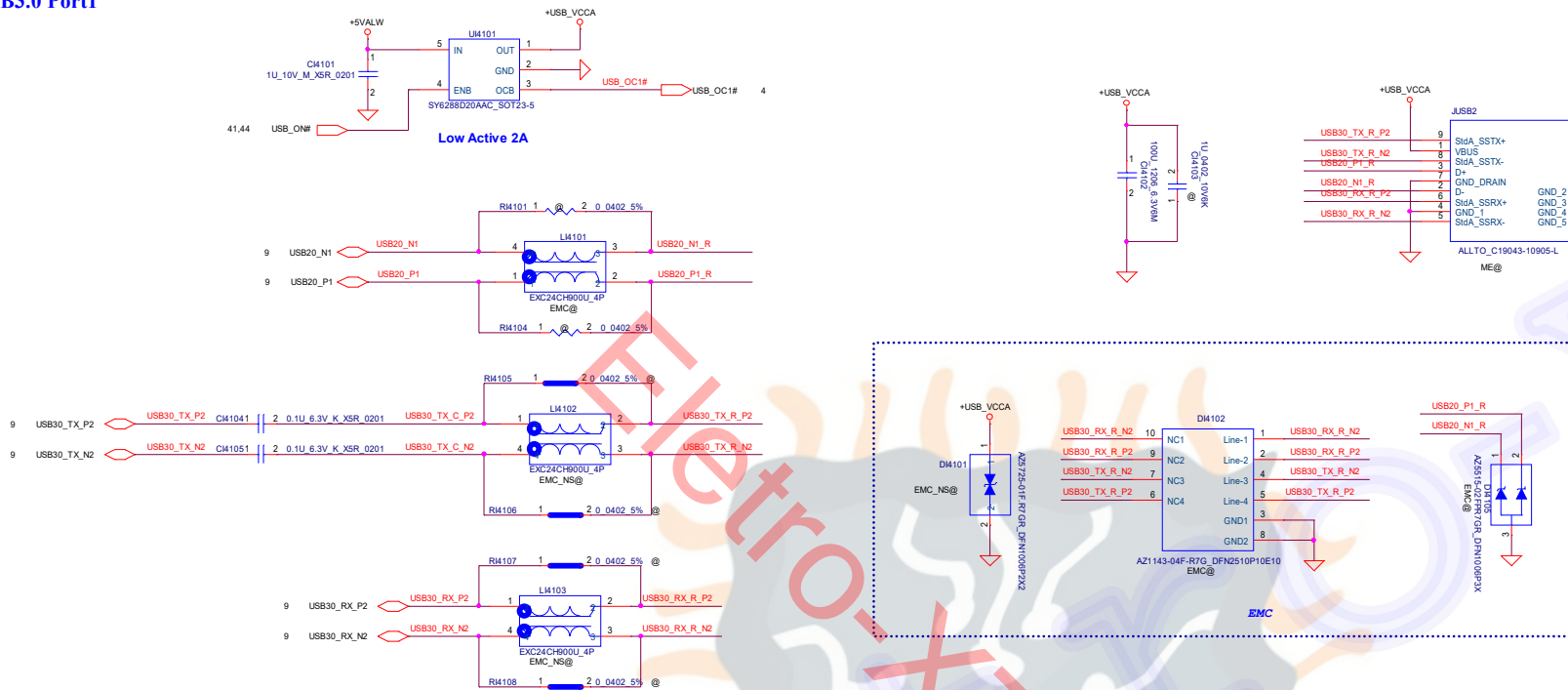


Eletro-X

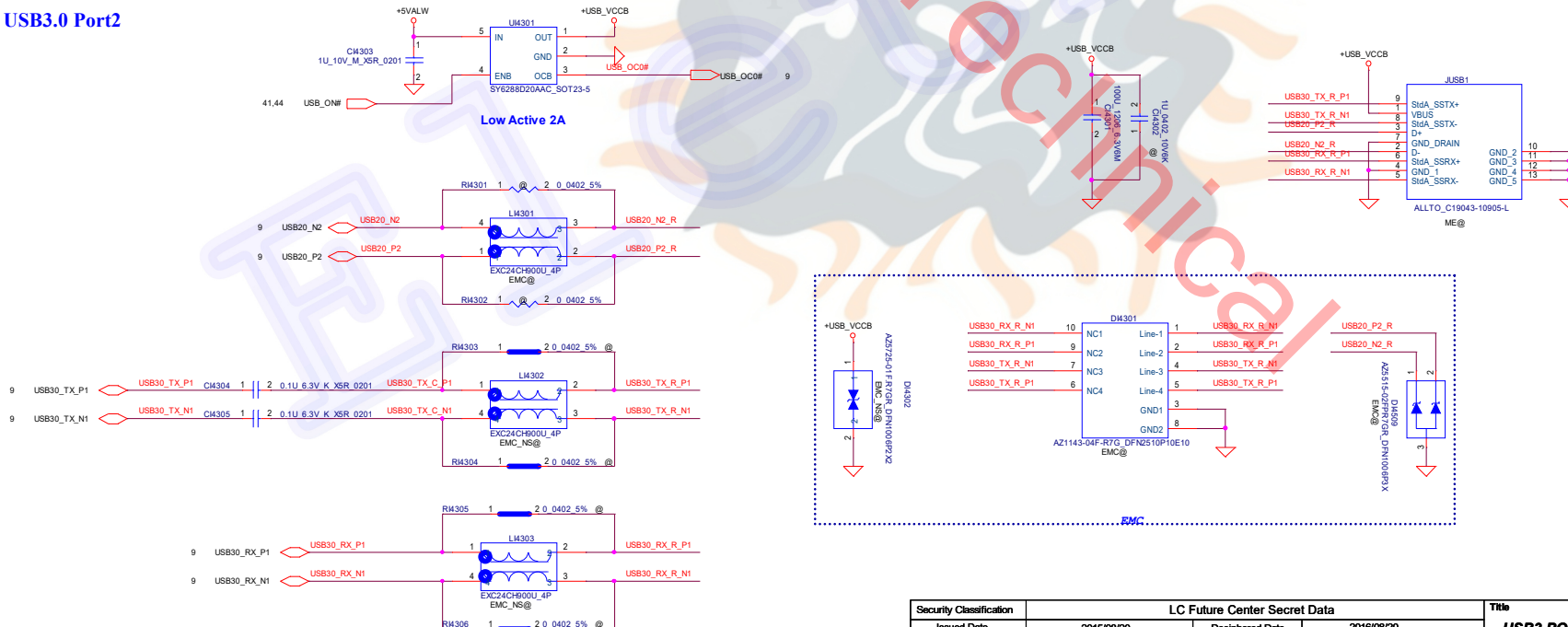


Security Classification		LC Future Center Secret Data		Title					
Issued Date		2016/12/14		Deciphered Date				2017/12/13	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RAD DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.									
Size		Document Number		Date		Rev			
		GS44D/GS54D		Friday, December 06, 2019		6.1			
				Sheet		40 of 60			

USB3.0 Port1

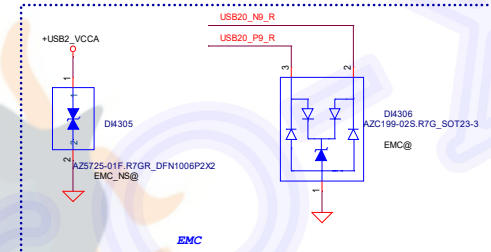
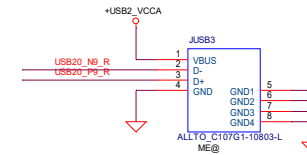
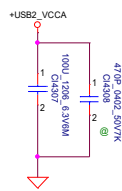
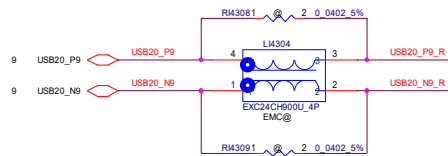
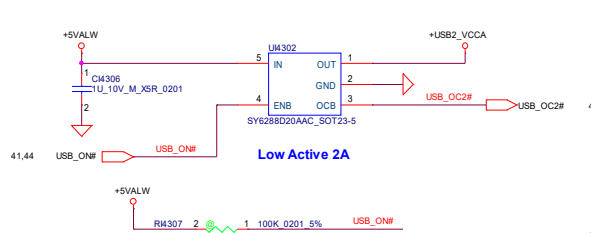


USB3.0 Port2



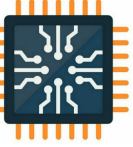
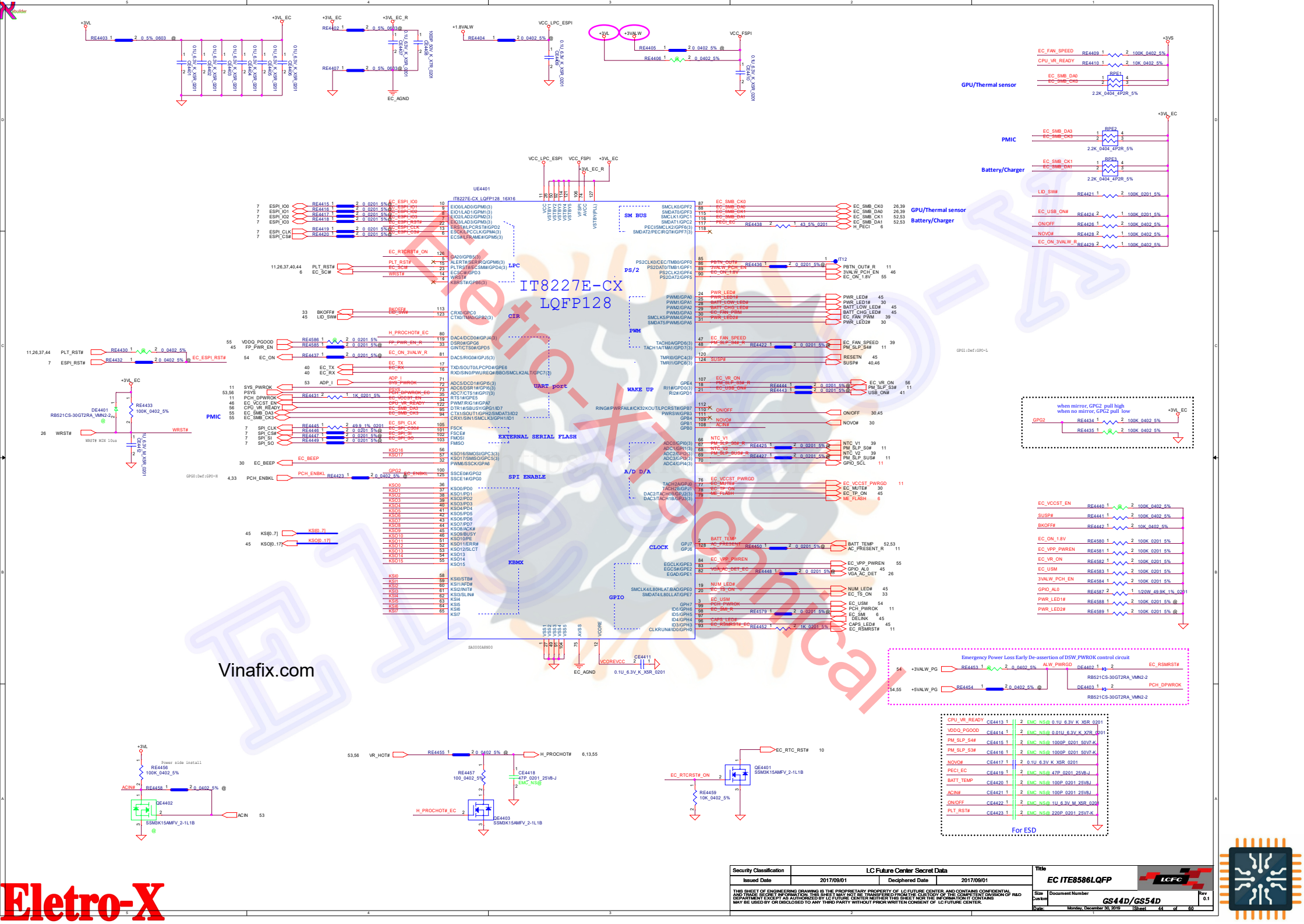
Security Classification	LC Future Center Secret Data		Title	USB3 PORT_LEFT	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Size	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				GS44D/GS54D	
				Date	Friday, December 06, 2018
				Sheet	41 of 60
				Rev	0.1

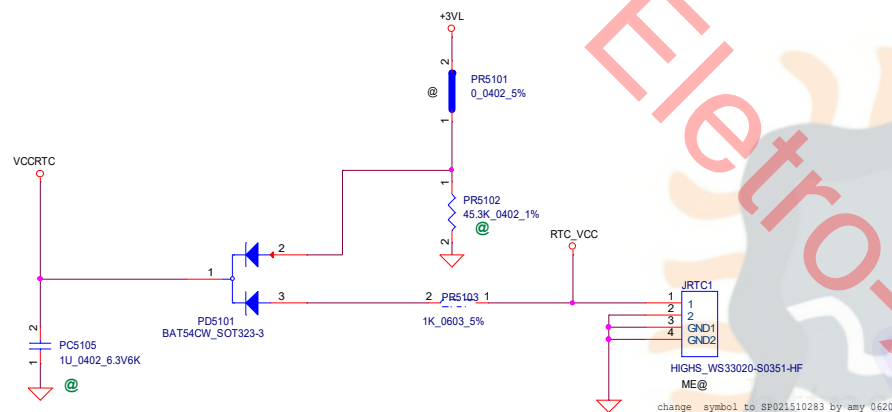
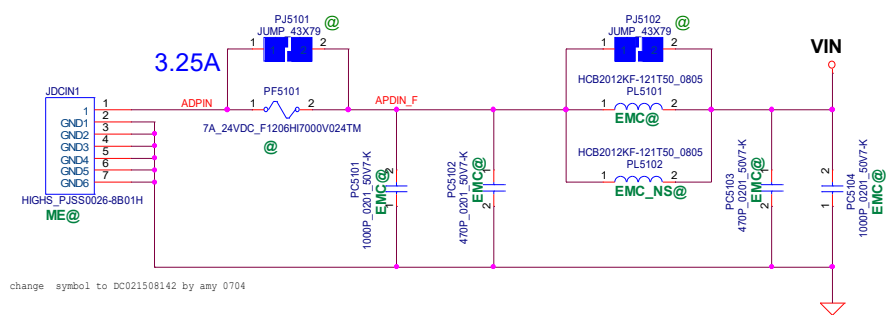
USB2.0 PORT x1



Security Classification	LC Future Center Secret Data		Title	USB3 Port_Right & USB2.0	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Size	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				GS44D/GS54D	Rev 0.1
				Date: Friday, December 06, 2018	Sheet 42 of 60



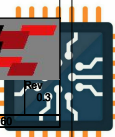


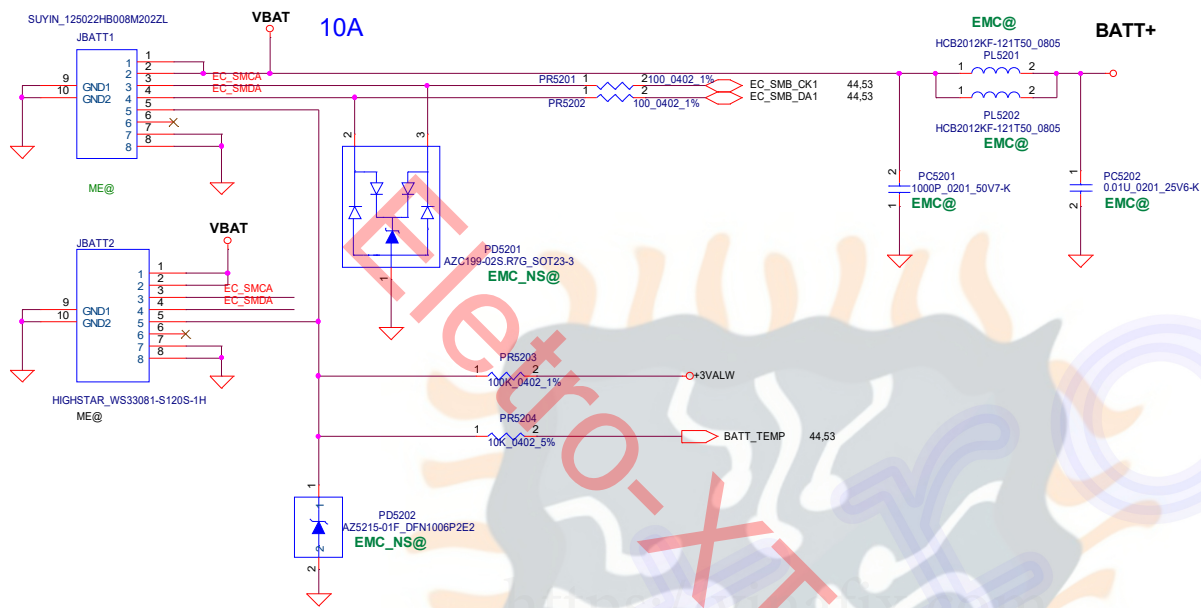


RTC_VCC 20MIL
+3V_L 20MIL
VCCRTC 20MIL

Security Classification	LC Future Center Secret Data	
Issued Date	2018/07/10	Deciphered Date
		2018/07/10
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.		

Title	
PWR-DCIN / RTC charger	
Size	Document Number
Custom	GS44D/GS54D
Date:	Friday, December 06, 2019
Sheet	51 of 6

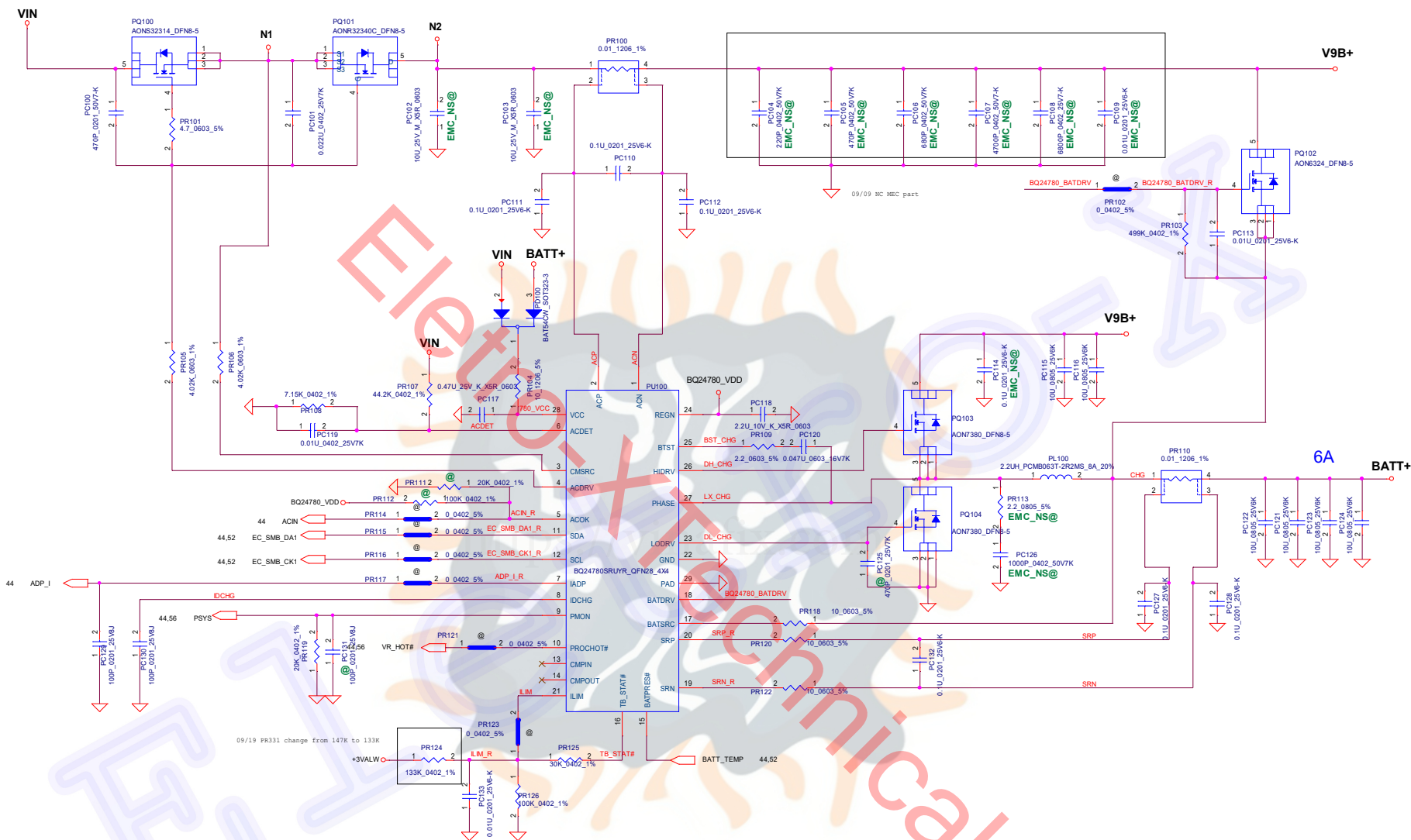




2S1P polymer battery
voltage level: +5.5V ~
8.8 V

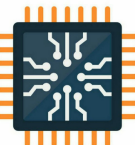
Security Classification		LC Future Center Secret Data	
Issued Date	2018/07/10	Deciphered Date	2018/07/10
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.			

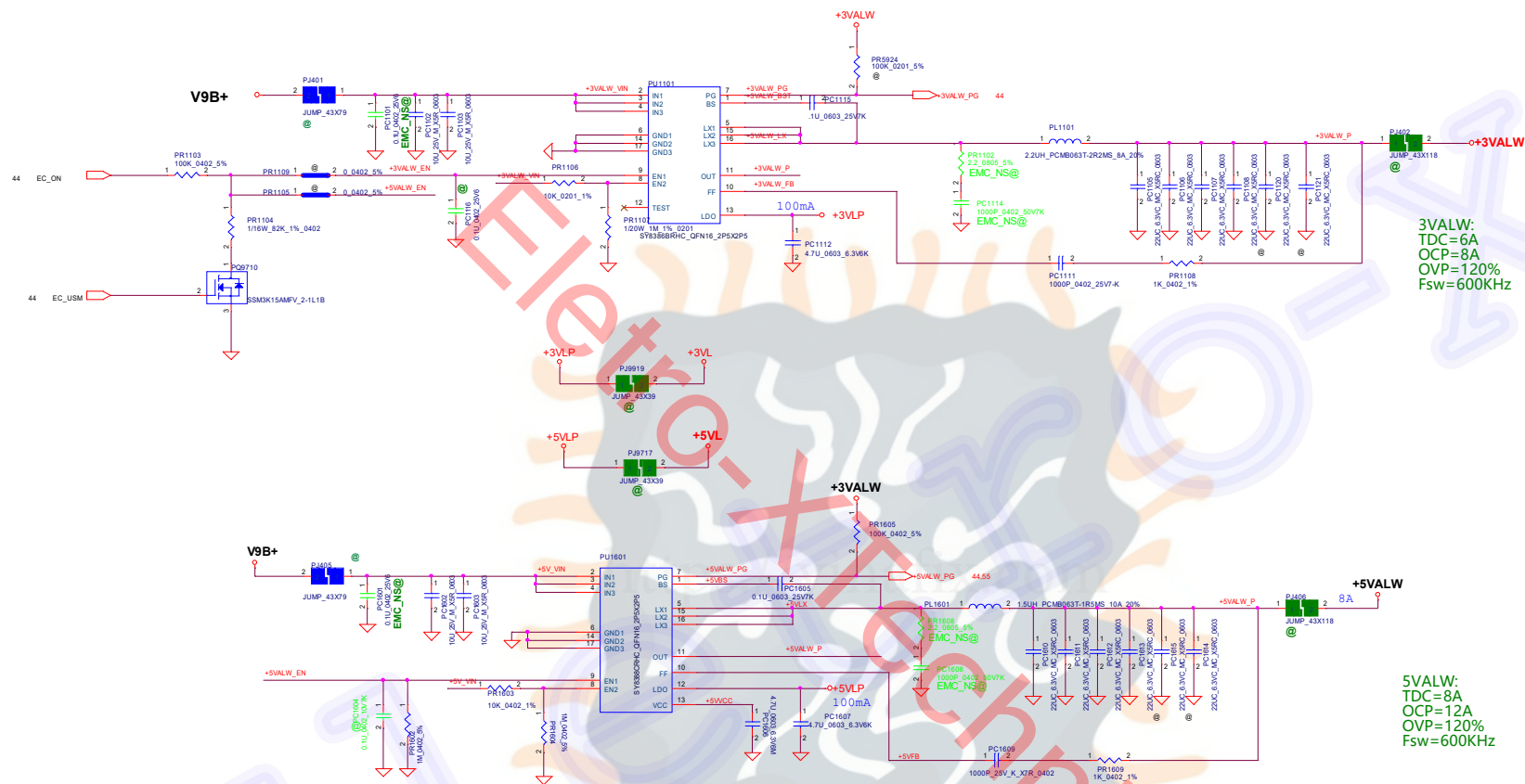
Title	
PWR-BATTERY CONN/OTF ICFC	
Size	Custom
Document Number	GS44D/GS54D
Date	Friday, December 06, 2019
Sheet	52 of 6

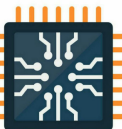
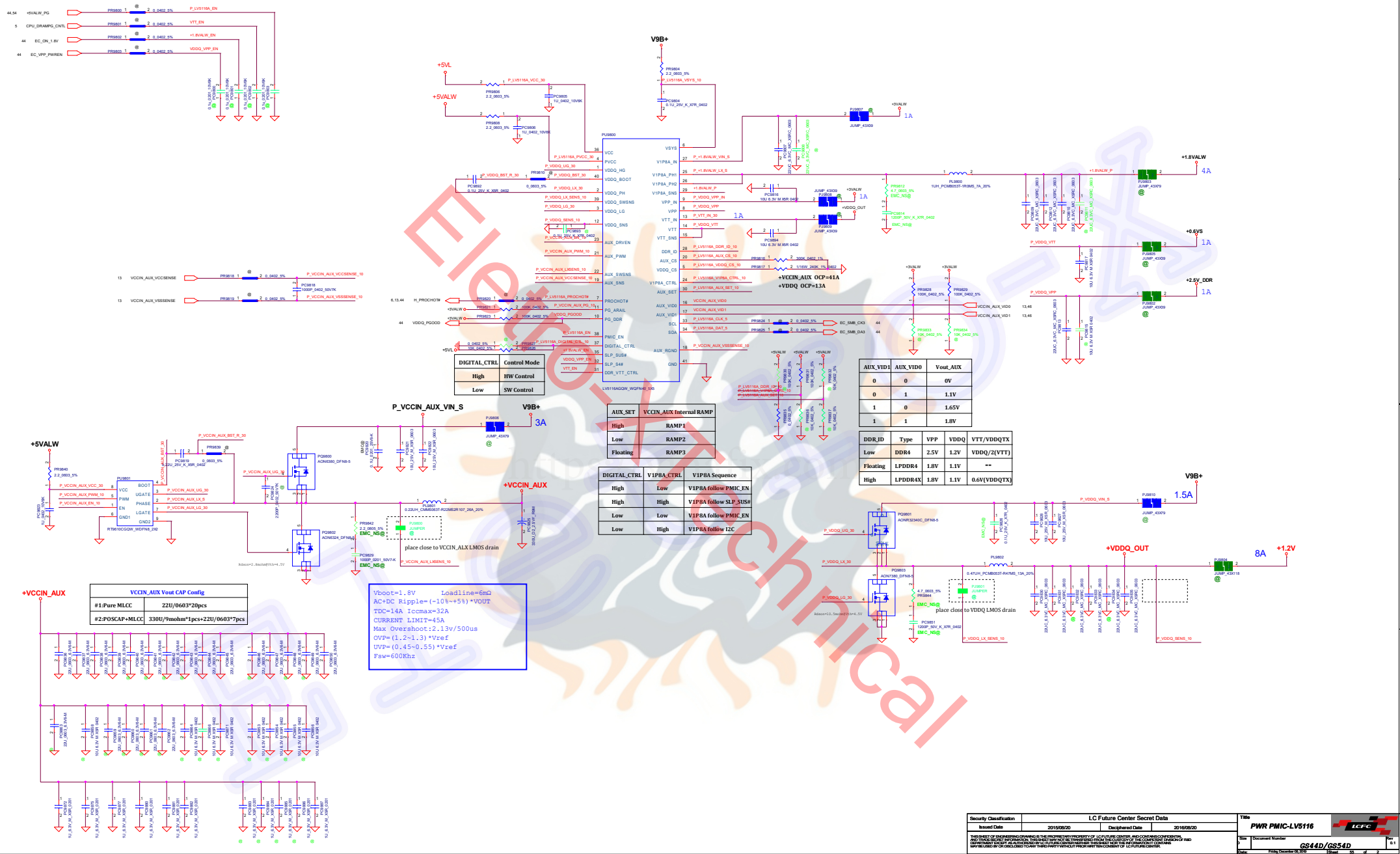


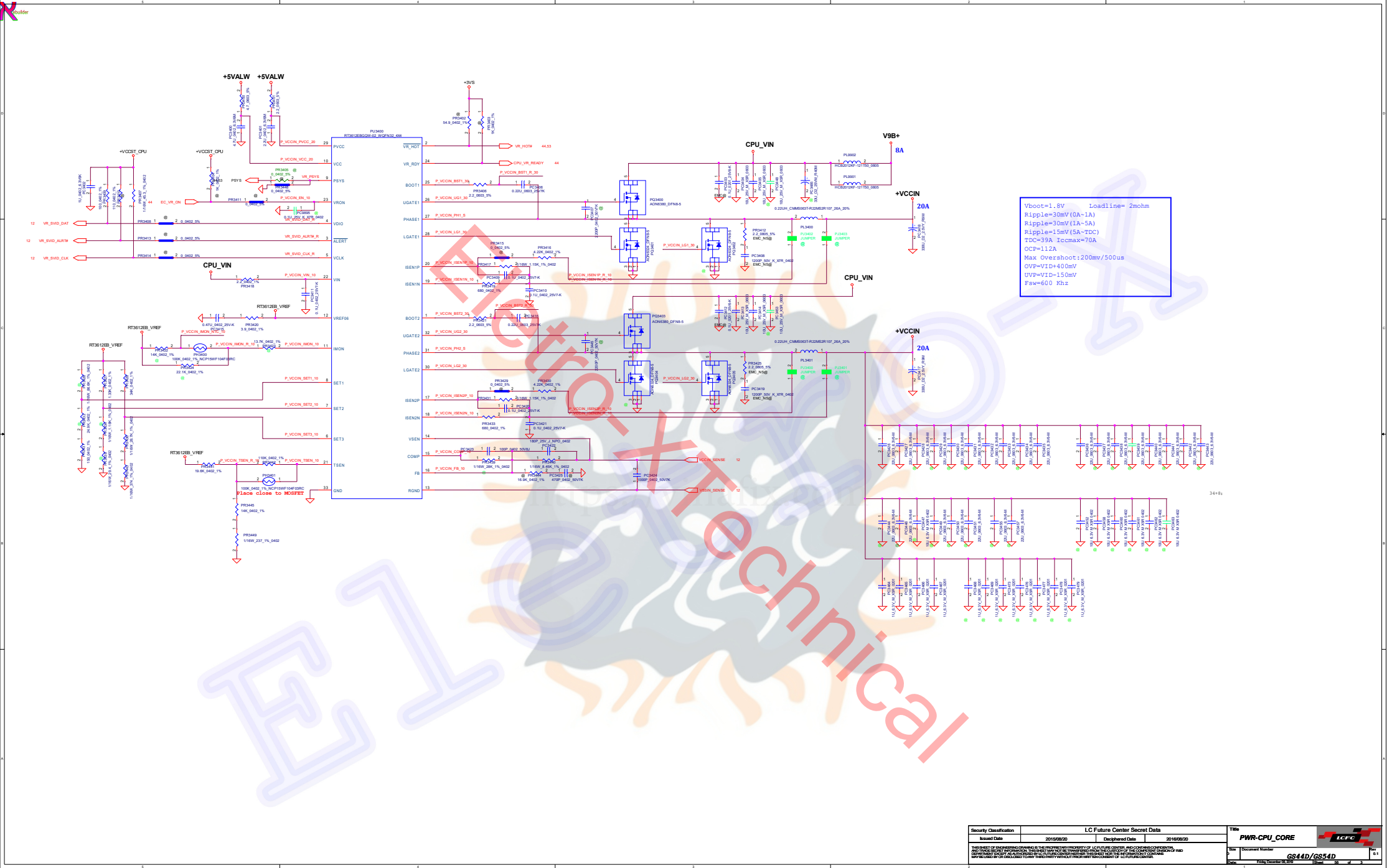
ACDECT setting 17.2V
 Charge current limit HW=7A
 DC discharge limit =26A
 Discharge current limit HW=9A during Turbo boost

Security Classification		LC Future Center Secret Data		Title						
Issued Date		2018/07/10	Deciphered Date	2018/07/10						
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</p>										
						Size		Document Number		Rev
						C		GS44D/GS54D		0.3
						Date:		Friday, December 06, 2019		Sheet
								53		of 1

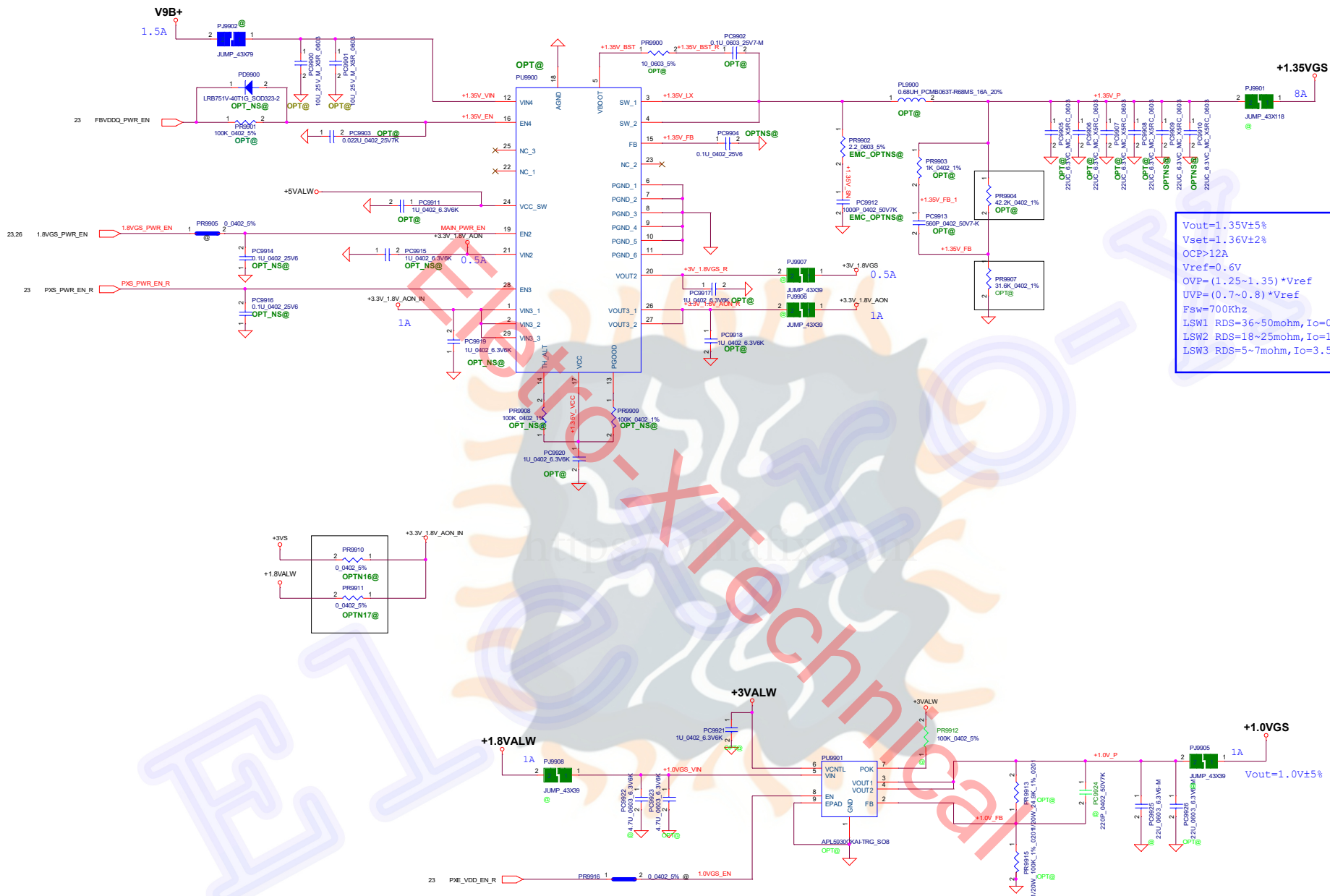








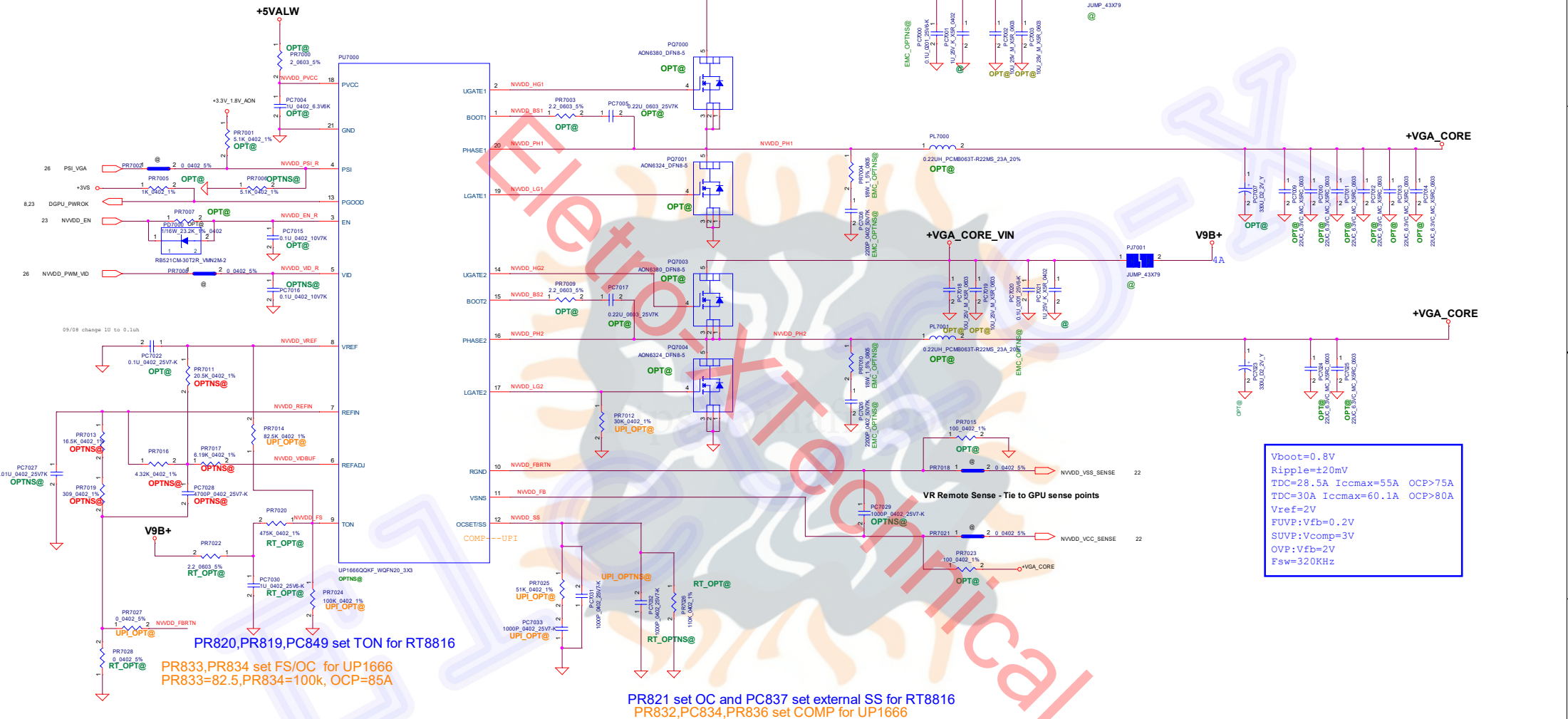
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2019/08/29	Designed Date	2019/08/29	PWR-CPU_CORE	
<div>THIS IS THE BEST OF THE FUTURE CENTER'S PROPERTY. IT IS THE PROPERTY OF THE FUTURE CENTER AND IS NOT TO BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM. ANY UNAUTHORIZED REPRODUCTION OR TRANSMISSION OF THIS DOCUMENT IS STRICTLY PROHIBITED. THE FUTURE CENTER ASSUMES NO LIABILITY FOR ANY DAMAGE OR LOSS OF DATA ARISING FROM THE USE OF THIS DOCUMENT. THE FUTURE CENTER IS NOT RESPONSIBLE FOR ANY CONSEQUENCES ARISING FROM THE USE OF THIS DOCUMENT. THE FUTURE CENTER IS NOT RESPONSIBLE FOR ANY CONSEQUENCES ARISING FROM THE USE OF THIS DOCUMENT.</div>					
Rev	01	Document Number	GS44D/GS54D		
Date	2019/08/29	Page	55	of	5



Vout=1.35V±5%
Vset=1.36V±2%
OCP>12A
Vref=0.6V
OVP=(1.25~1.35)*Vref
UVP=(0.7~0.8)*Vref
Fsw=700Khz
LSW1 RDS=36~50mohm, Io=0.5A
LSW2 RDS=18~25mohm, Io=1A
LSW3 RDS=5~7mohm, Io=3.5A

PWM-VID Specification			
	N17 Config	N16 Config B	
Vmin(V)	0.3	0.6	
Vmax(V)	1.3	1.2	
Vboot(V)	0.8	0.9	
Vstep(mV)	6.25	6.25	
N(level)	160	96	
Fpwm(KHz)	675	1.125	
Tdmin(nS)	9.26	9.26	
T(uS)	<100	<100	

RT8816 PSI	UPL666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM

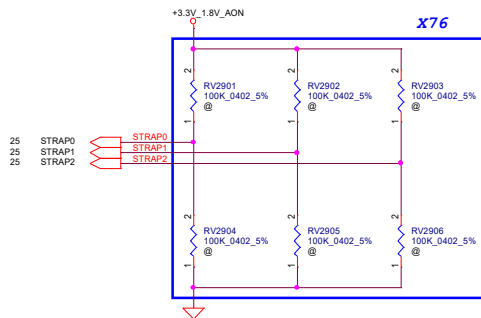


Component	Value	N17	N16
R1 (KΩ)	PR7017	6.19	20
R2 (KΩ)	PR7011	20.5	20
R3 (KΩ)	PR7016	4.32	2
R4 (KΩ)	PR7013	16.5	18
R5 (KΩ)	PR7019	0.309	0
C (nF)	PC7028	4.7	2.7

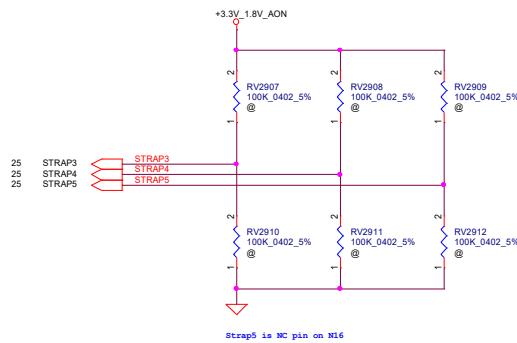
UPL_OPT@ : for UPL666
 RT_OPT@ : for RT8816A

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	PWR-VGA_CORE	
THIS IS A SET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THE SHEET MAY NOT BE TRANSMITTED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE REPRODUCED OR DISCLOSED TO ANY THIRD PARTY WITHOUT THE WRITTEN CONSENT OF LC FUTURE CENTER.				Size Custom	Document Number GS44D/GS54D
				Date	Friday, December 06, 2019
				Sheet	58 of 4





GPU	FB Memory (GDDR5)	RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
8Gb	Samsung 8Gb	K4G80325FB-HC28	0 (0x0000)	L	L
	Micron 8Gb	MT51J256M32HF-70:A	1 (0x0001)	L	L
	Hynix 8Gb	H5GC8H24MJR-R0C	2 (0x0010)	L	H



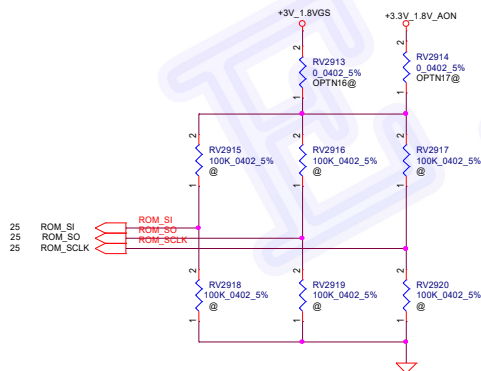
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGINAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE



	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N17S-G1	H	H	M	0000
N16S-GTR				

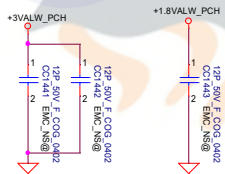
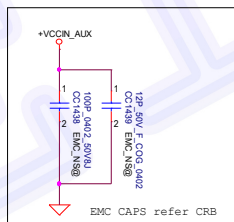
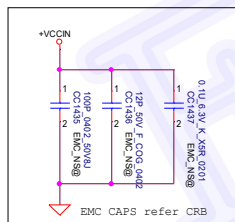
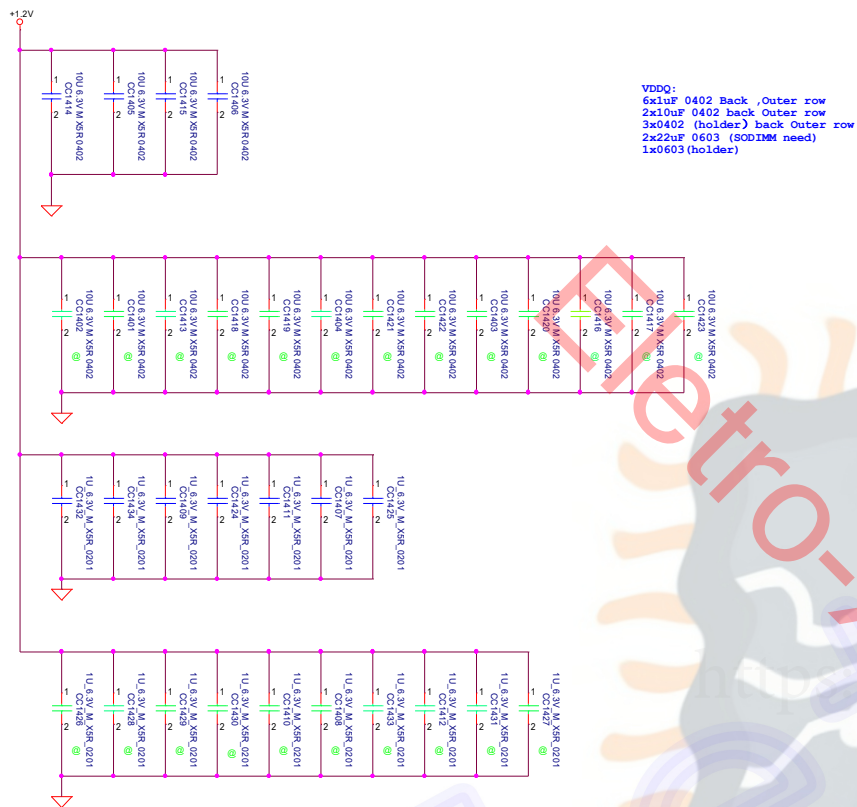
1: ENABLE 0: DISABLE
SOR0/1/2/3 DISABLE

DEVID_SEL
0 (Default)
1

PCIE_CFG
0 (Default)
1

SMBUS_ALT_ADDR
0 0x9E (Default)
1 0x9C (Multi-GPU usage)

VGA_DEVICE
0 3D Device (Class Code 302h)
1 VGA Device (Default)

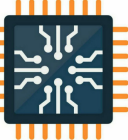
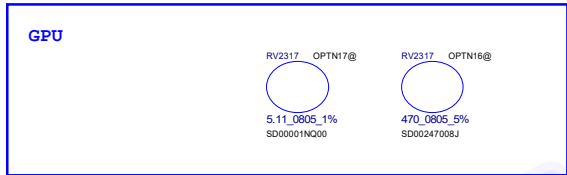
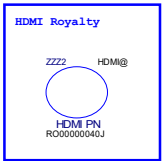
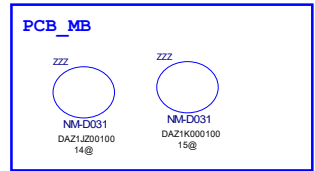
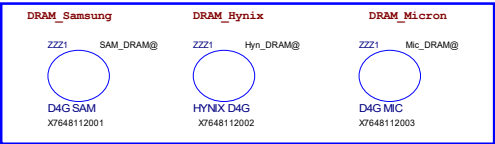
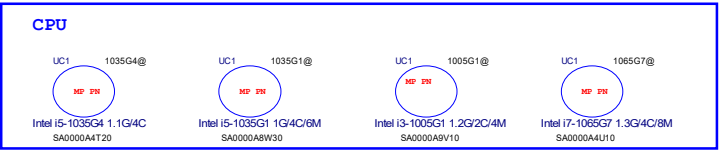


POWER

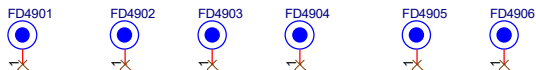
U42@ PR3423 13.7K ±1% 0402 SD03413728J	U42@ PR3424 22.1K ±1% 0402 SD03422128J	U42@ PR3422 14K ±1% 0402 SD03414028J	U42@ PR3439 28K ±1% 0402 SD000015J00	U42@ PR3426 86.6K ±1% 0402 SD00001PM00	U42@ PR3432 24.9K ±1% 0402 SD03424928J	U42@ PR3434 1.18K ±1% 0402 SD00001D000	U42@ PR3438 29.4 ±1% 0402 SD00001BC00
U22@ PR3423 20.5K ±1% 0402 SD03420528J	U22@ PR3424 25.6K ±1% 0402 SD03425528J	U22@ PR3422 11.5K ±1% SD03411528J	U22@ PR3439 24.3K ±1% SD000011300	U22@ PR3426 130K ±1% 0402 SD03413038J	U22@ PR3432 22.6K ±1% 0402 SD000019W00	U22@ PR3434 1.1K ±1% 0402 SD03411018J	U22@ PR3438 40.2 ±1% 0402 SD034402A8J

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2018/08/20	Deciphered Date	2016/08/20	POWER CHANGE LIST	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Scale	Document Number
				GS44D/GS54D	
				Date	Tuesday, December 10, 2019
Sheet	59	of	62	Rev	0.1

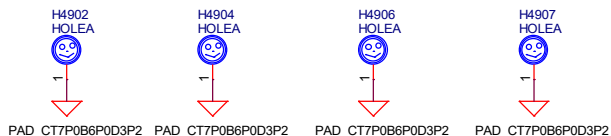




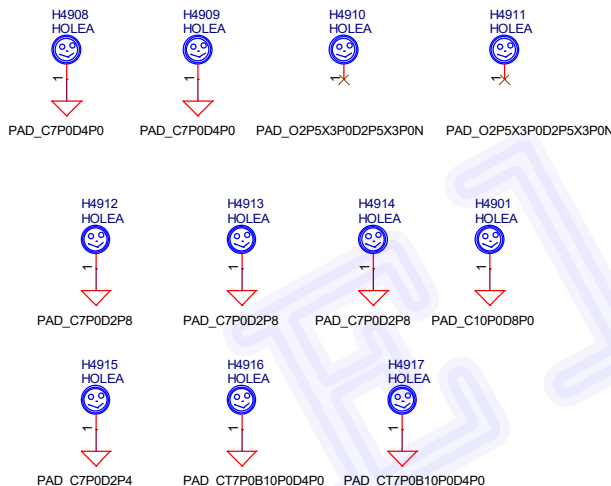
PCB Fedcal Mark PAD



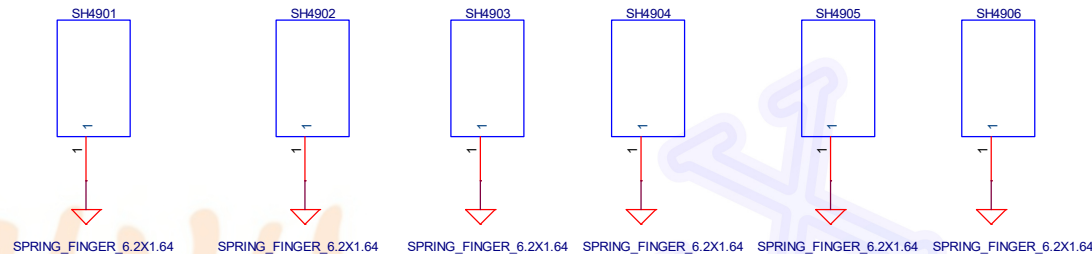
CPU Thermal Hole



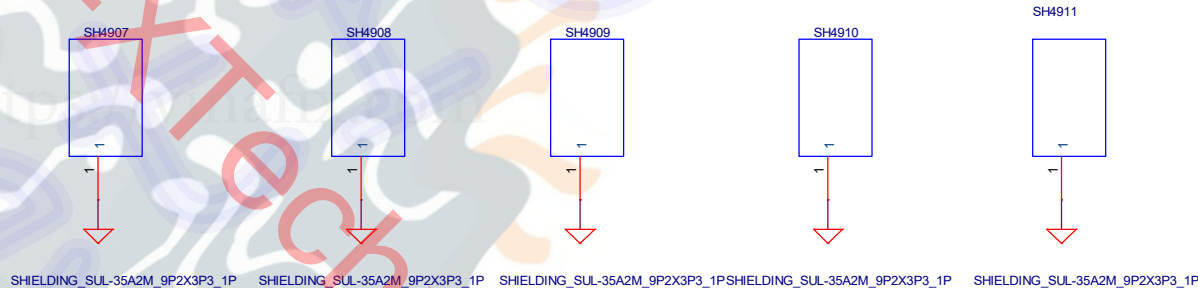
GPU Thermal Hole




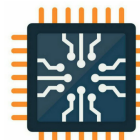
MD Shielding



SODIMM Shielding



Security Classification	LC Future Center Secret Data			Title	Hole	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Document Number		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					Rev	0.1
					Date:	Friday, December 06, 2019
					Sheet	49 of 60



N16x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU Core VDD PWM control signal
GPIO1	OUT	N/A	FB Enable for GC6 2.0
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT		FBVREF_ALTV for GDDR5
GPIO11	OUT	-	
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

Products	GPU (W)	Mem (W)	Min Core Clk (MHz)	NVVDD (V)			FBVDD (1.35V) (W)		FBVDDQ (GPU+Mem) (1.35V) (W)		(1.05V) (6) (mA)		Other (3.3V) (mA)	
N16S-GMR	16	1.6	849	TBD	19	TBD	2	TBD	4.2	TBD	800	TBD	60	TBD
N16S-GTR	18	1.7	967		26.5		2		4.2		800		60	

N16x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

